Compal Confidential

KAV10 Schematics Document

Intel Diamondville Processor with Calistoga(945GSE) + DDRII + ICH7M

2009-01-21

REV: 1.0

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Title: SCHEMATIC MB A4781

Size: B | Document Number: 401639 | Rev: D

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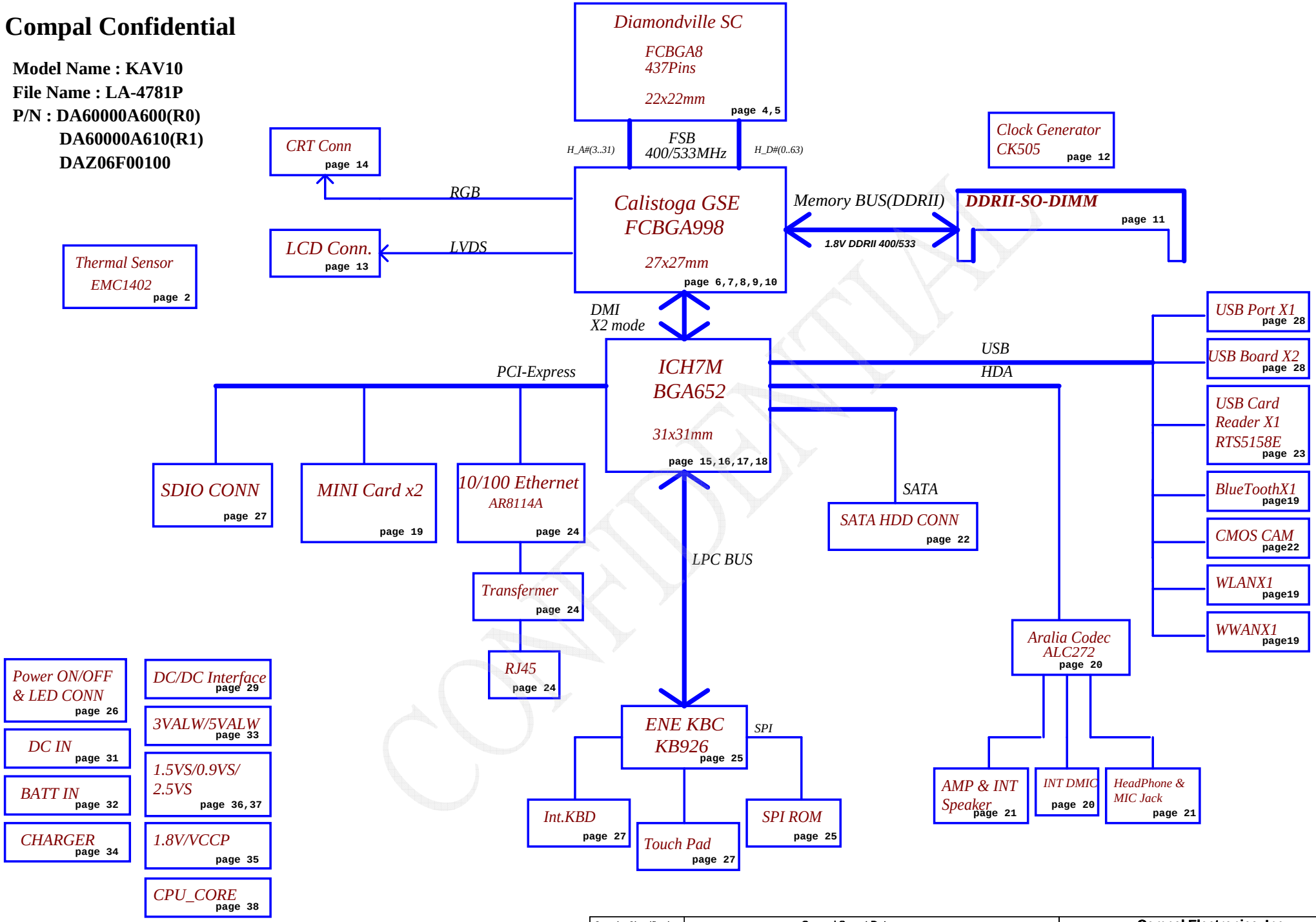
Model Name : KAV10
File Name : LA-4781P
P/N : DA60000A600(R0)
DA60000A610(R1)
DAZ06F00100



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+VCCP	VCCP switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table(Page 25)

ID	BRD ID	Ra	Rb	Vab
0	R01 (EVT)	NC	0	0V
1	R02 (DVT)	100K	8.2K	0.25V
2	R03 (PVT)	100K	18K	0.50V
3	R10A (MP)	100K	NC	3.3V

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ

No PCI Device

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b

EC SM Bus2 address

Device	Address
EMC1402	1001 100X b

ICH7M SM Bus address

Device	Address
Clock Generator (SLG8SP556VTR)	1101 001Xb
DDR DIMMA	1010 000Xb

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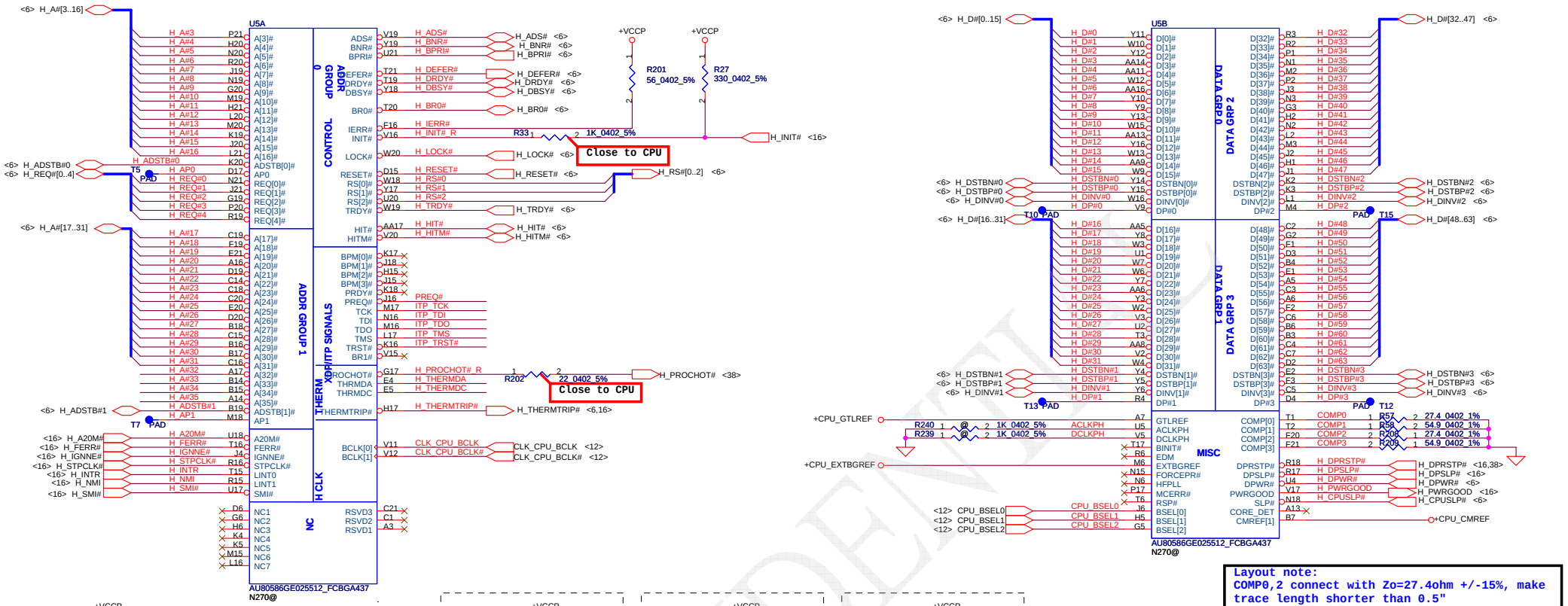
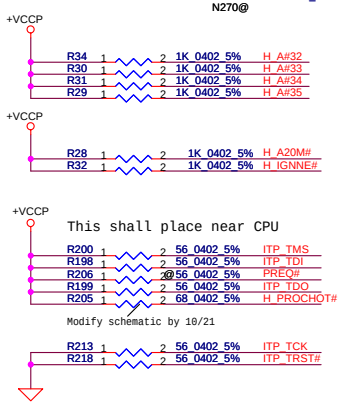
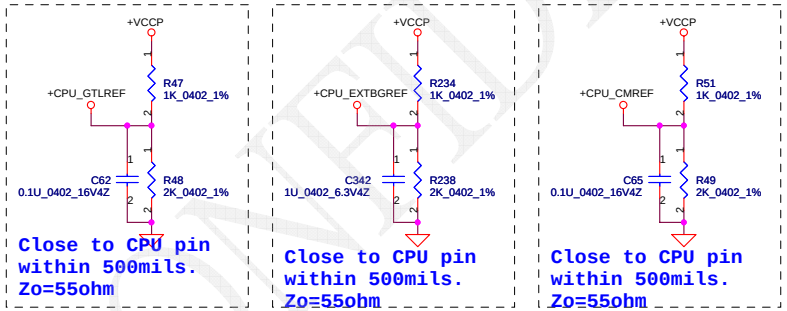
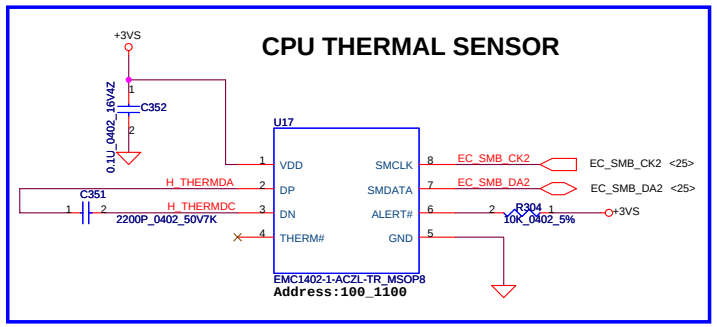


Layout note:
COMP0,2 connect with Zo=27.4ohm +/-15%, make trace length shorter than 0.5"
COMP1,3 connect with Zo=55ohm +/-15%, make trace length shorter than0.5"





H_THERMDA, H_THERMDC routing together.
Trace width / Spacing = 10 / 10 mil



U5
For N280 BOM
S IC AU80586GF028D SLGL9 C0 1.66G FCBGA 437P ABO !
N280@

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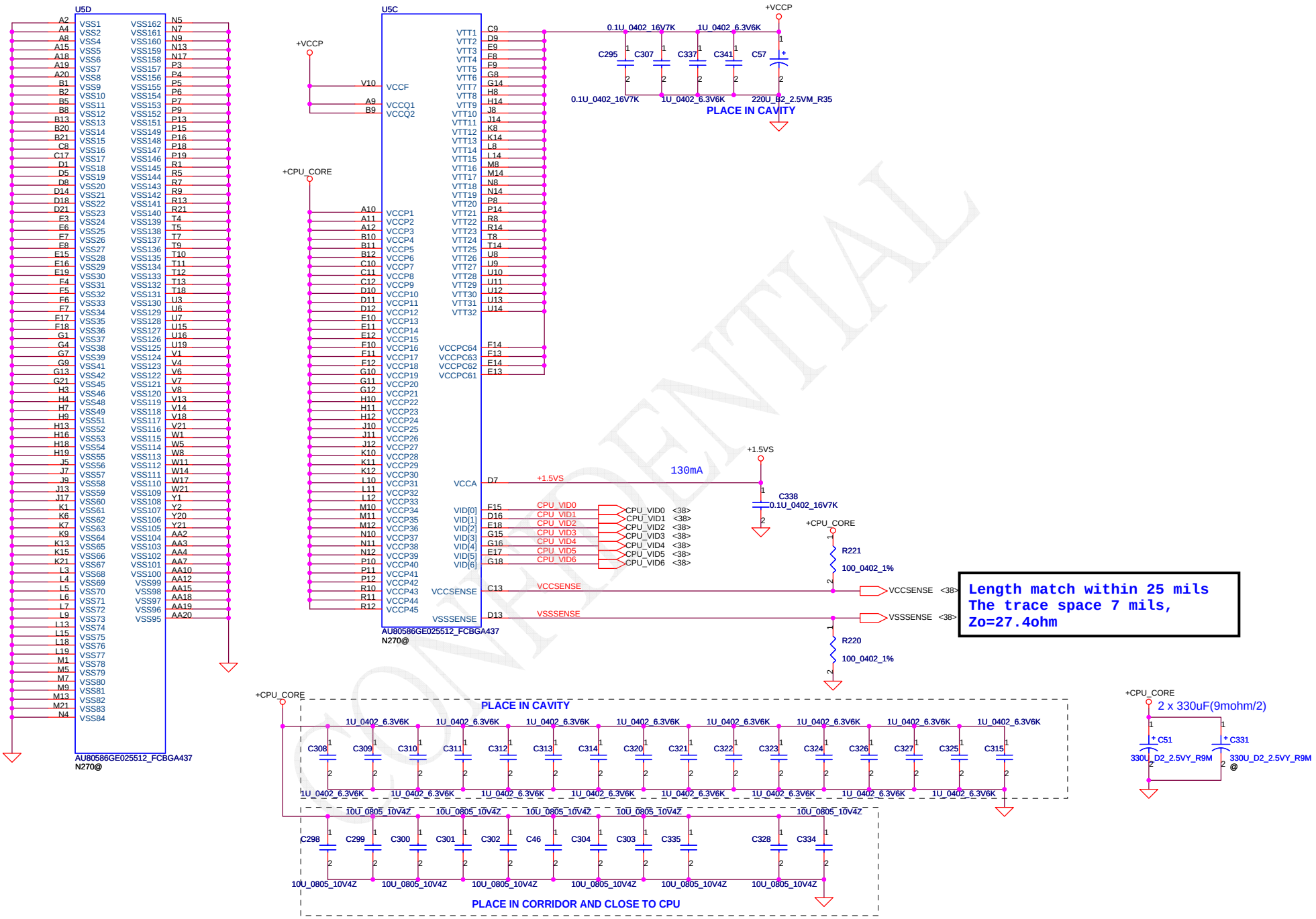

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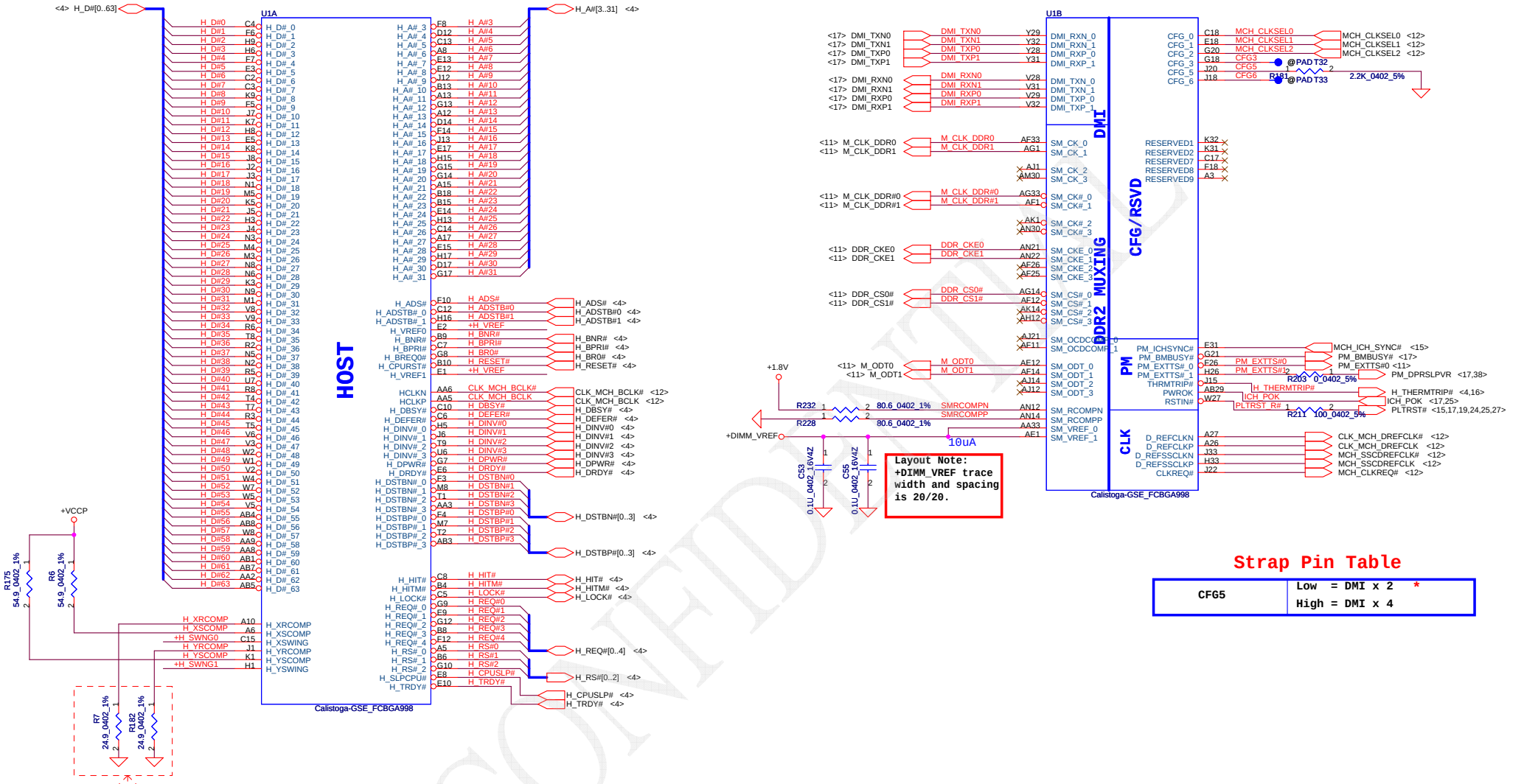

Strap Pin Table

CFG5	Low = DMI x 2 * High = DMI x 4

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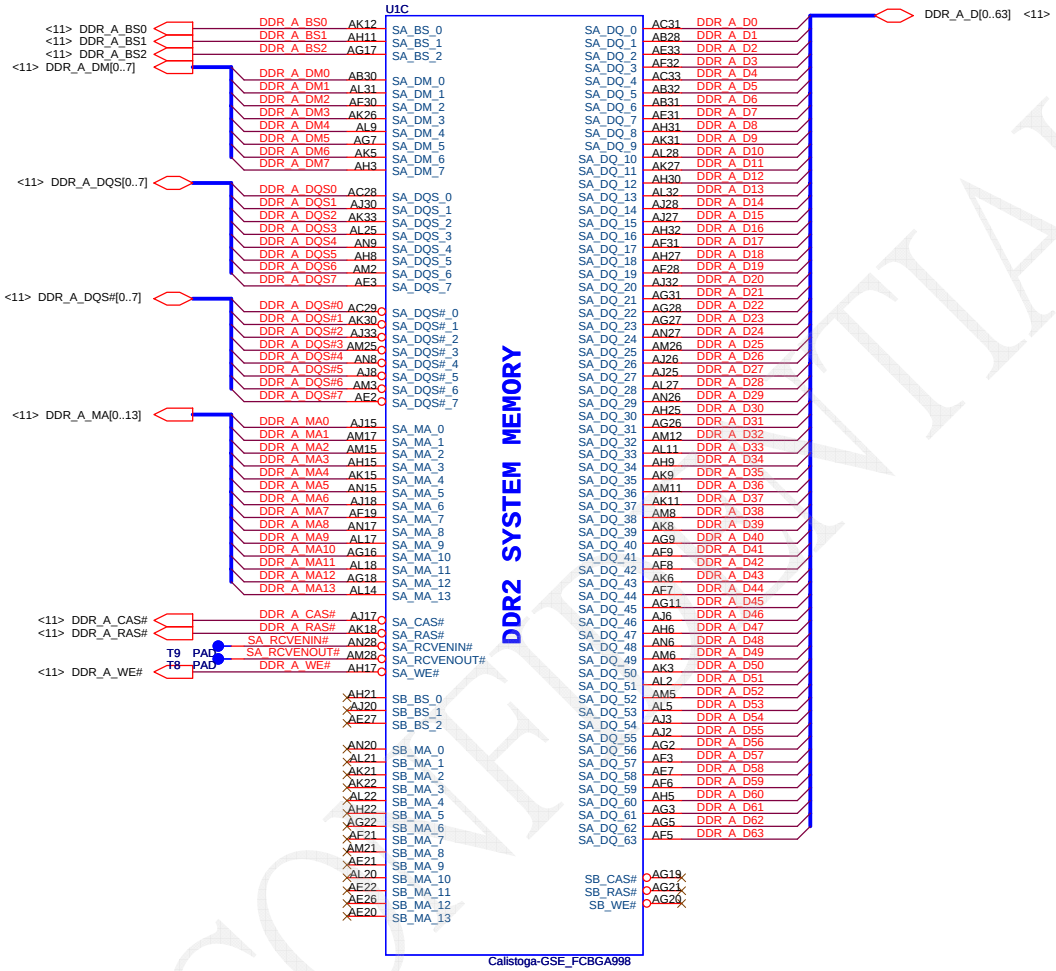

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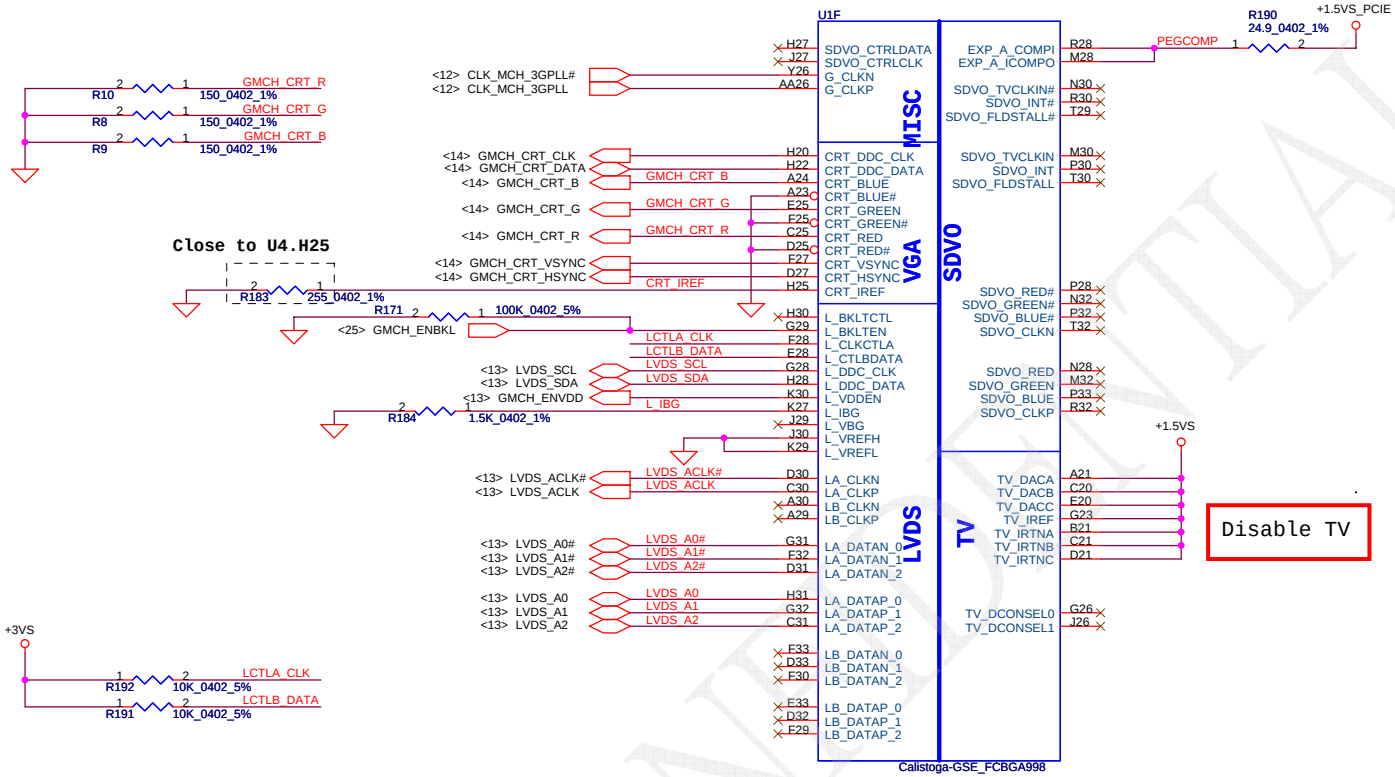

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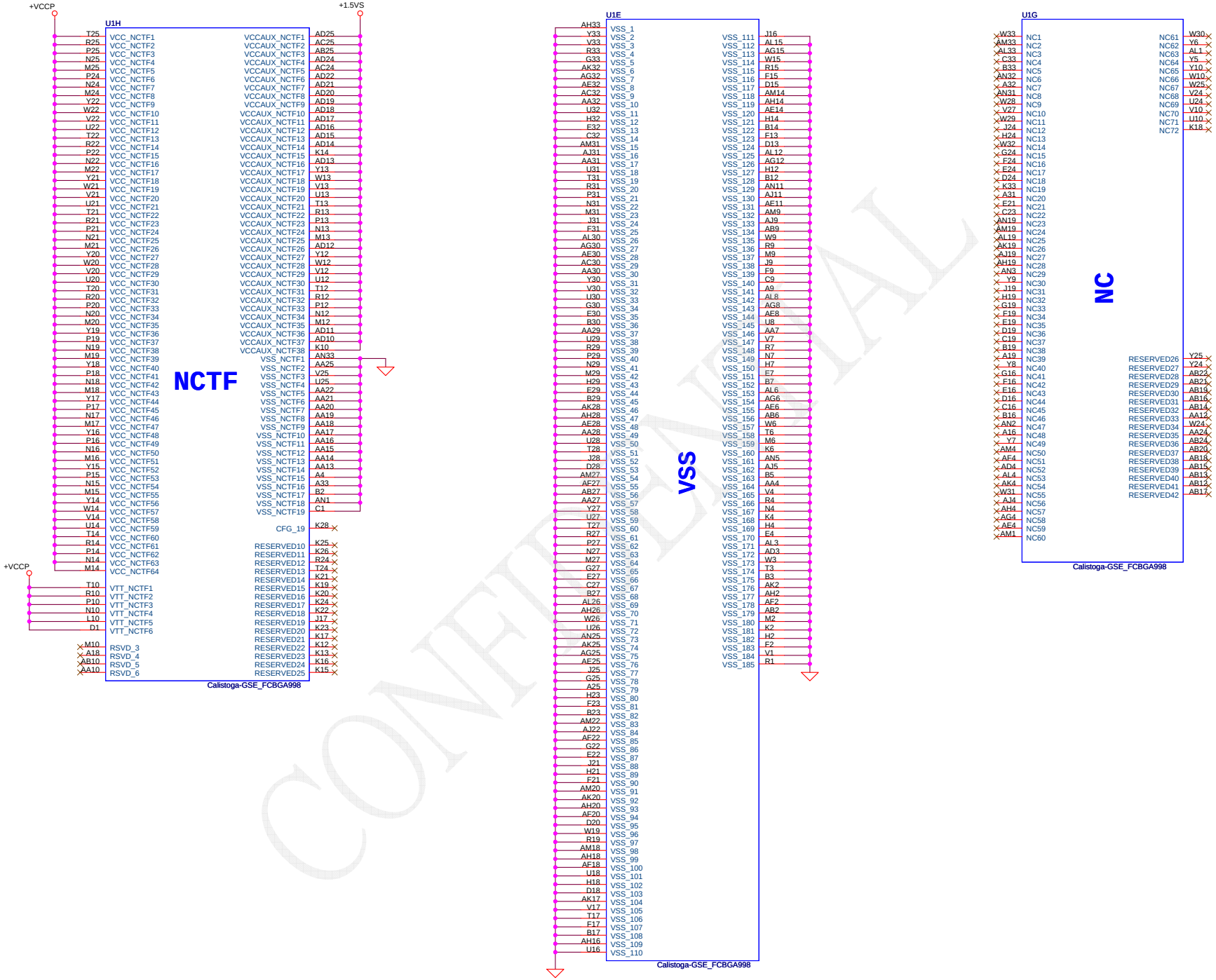

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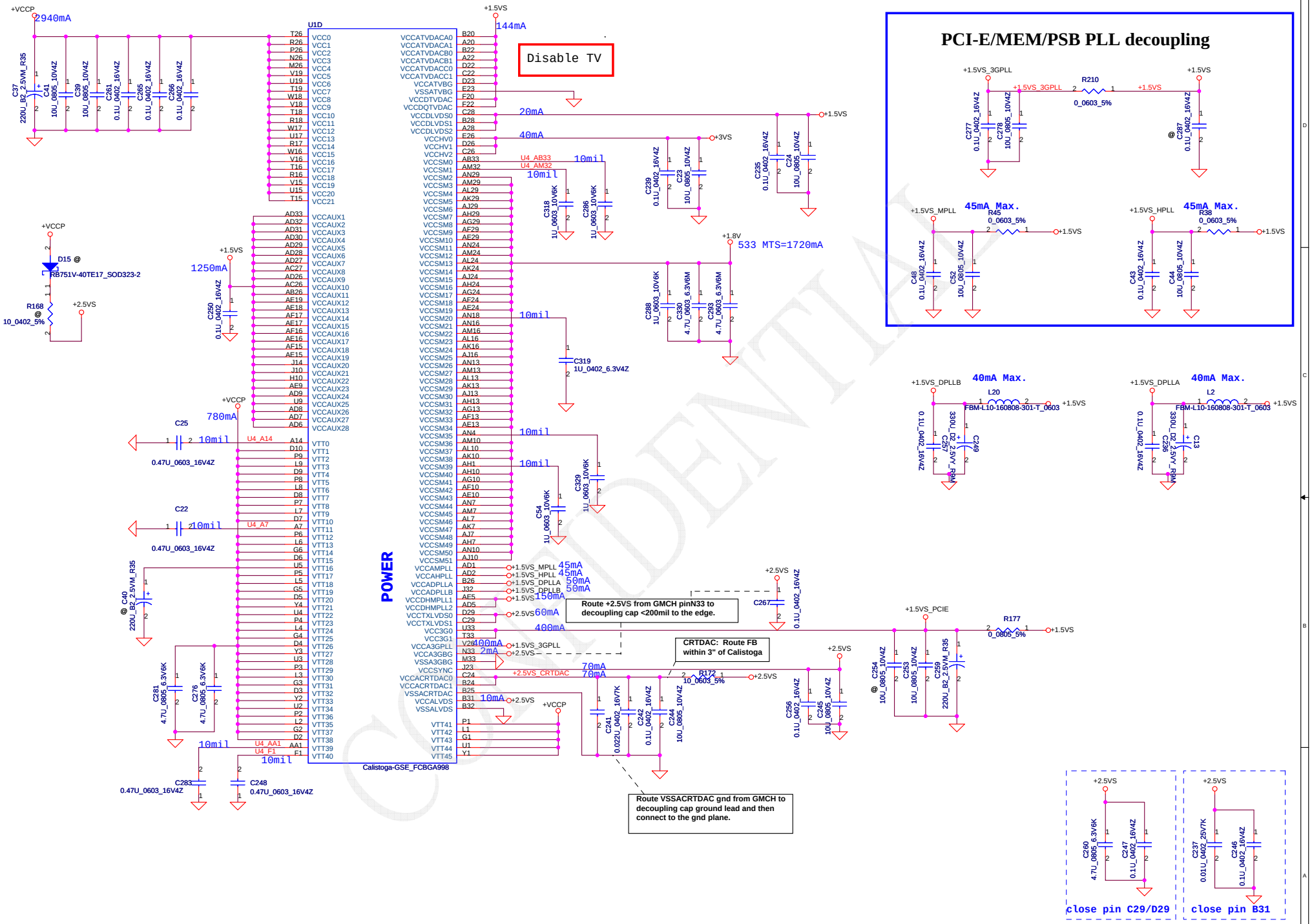

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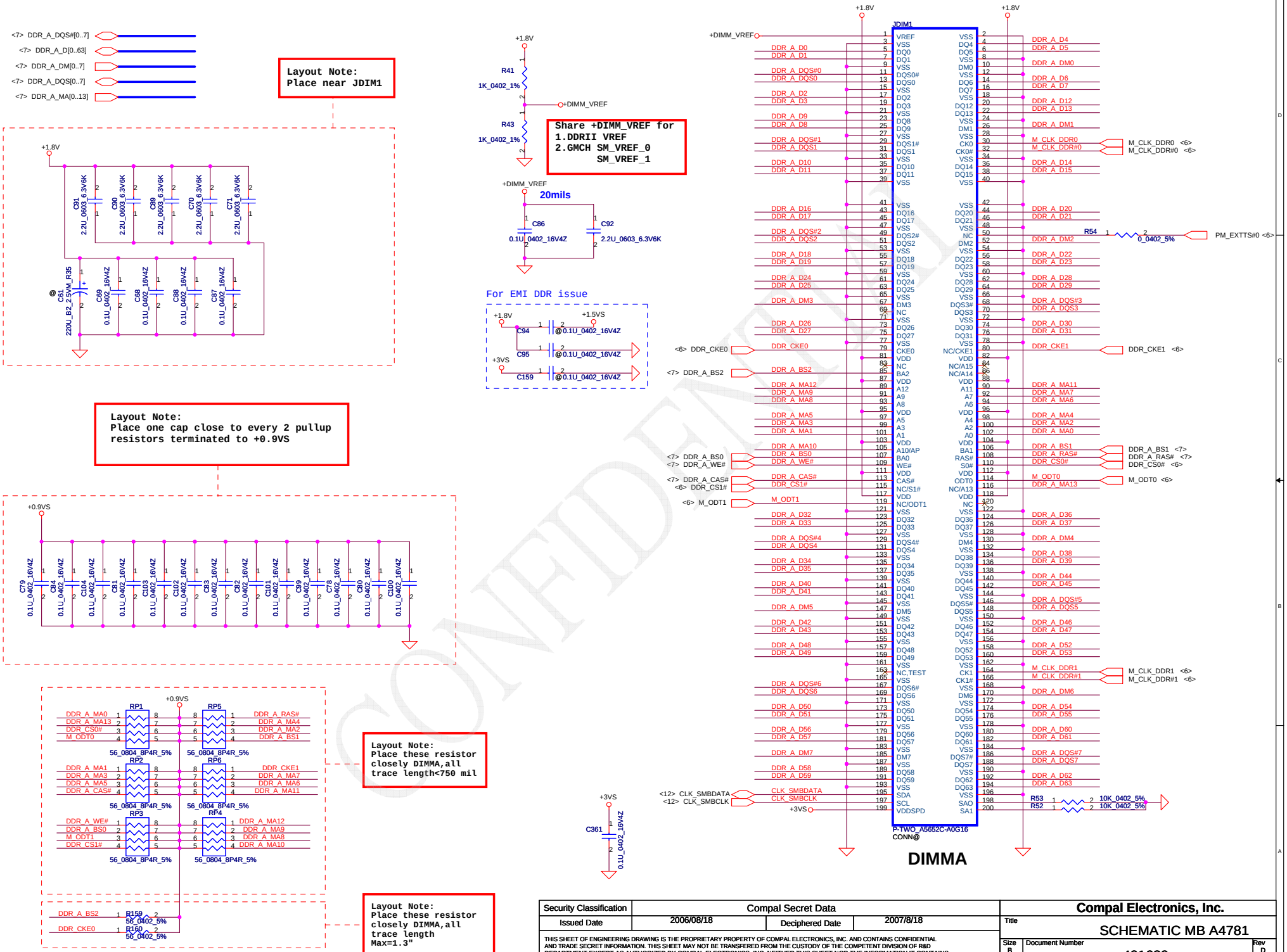
Layout Note:
Place near JDIM1
Share +DIMM_VREF for
1.DDRII VREF
2.GMCH SM_VREF_0
SM_VREF_1
20mils
For EMI DDR issue
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS
Layout Note:
Place these resistor closely DIMMA,all trace length<750 mil
Layout Note:
Place these resistor closely DIMMA,all trace length Max=1.3"
JDIM1
P-TWO_A5652C-A0G16
CONN@
DIMMA
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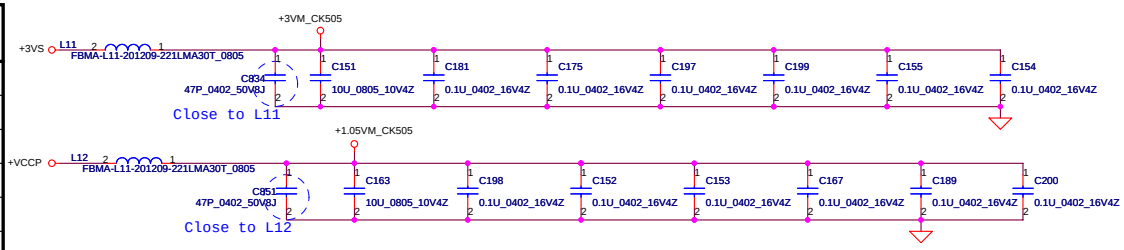
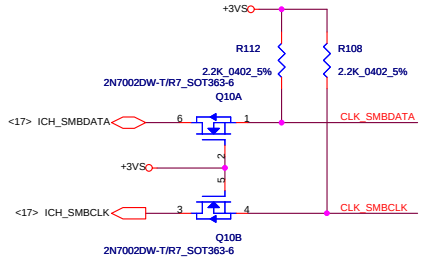
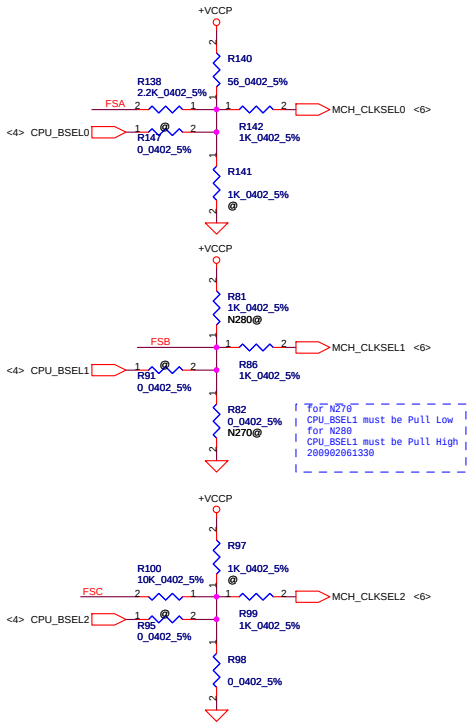
FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					

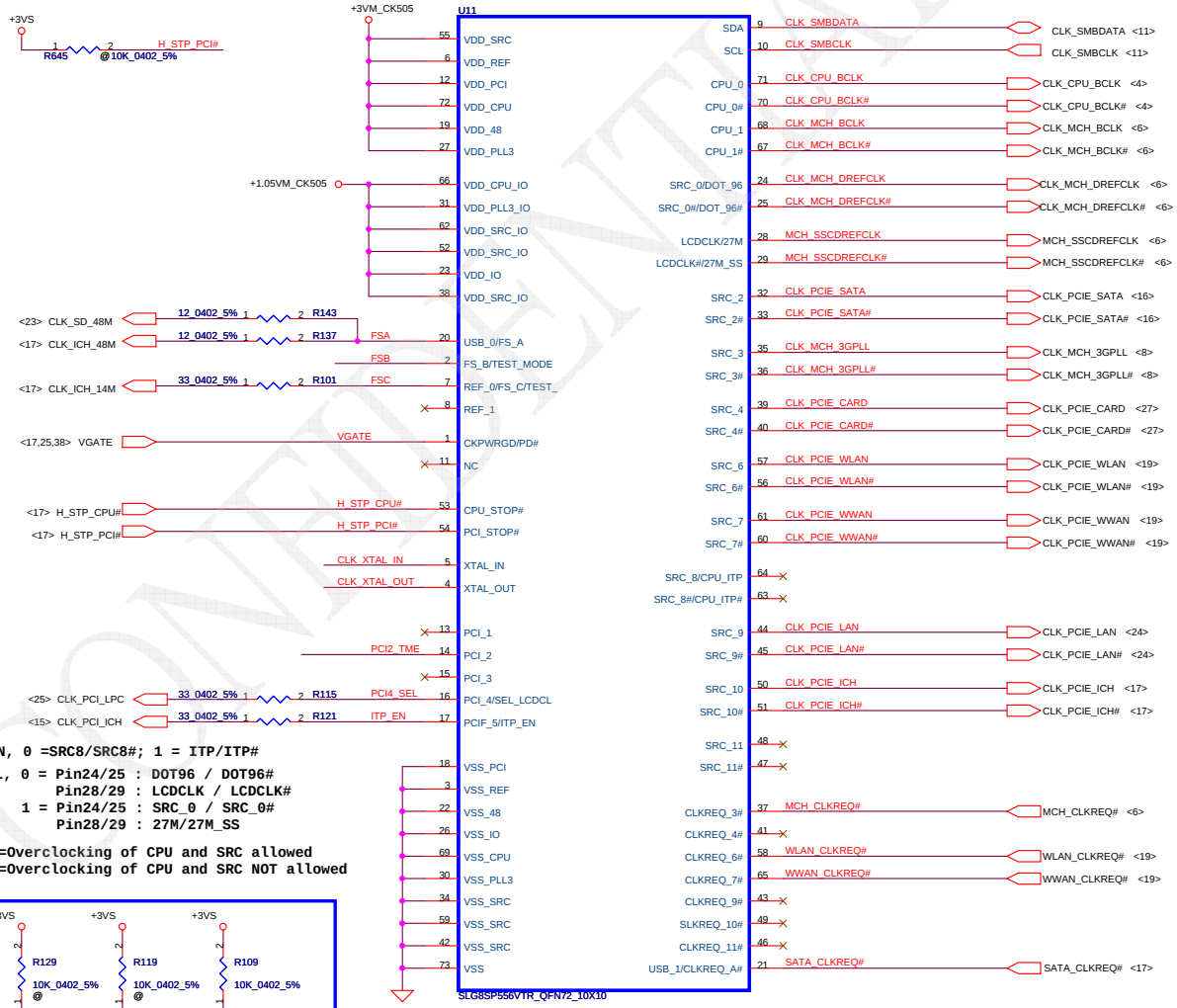




SA000020K00 (Silego : SLG8SP556VTR)

SA000020H10 (ICS : ICS9LPRS387AKLFT)

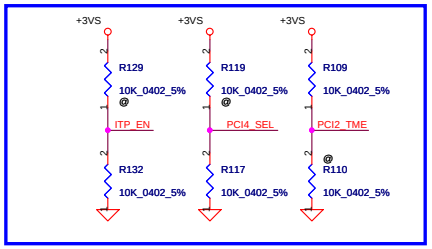




For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#

For PCI4_SEL, 0 = Pin24/25 : DOT96 / DOT96#
Pin28/29 : LCDCLK / LCDCLK#
1 = Pin24/25 : SRC_0 / SRC_0#
Pin28/29 : 27M/27M_SS

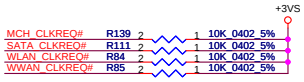
For PCI2_TME:0=Overclocking of CPU and SRC allowed
(ICS only) 1=Overclocking of CPU and SRC NOT allowed



Routing the trace at least 10mil

SRC PORT LIST

PORT	DEVICE
SRC0	MCH_DREFCLK
SRC2	SATA HDD
SRC3	MCH_3GPLL
SRC4	PCIE_CARDREADER
SRC6	PCIE_WLAN
SRC7	PCIE_WWAN
SRC8	
SRC9	PCIE_LAN
SRC10	PCIE_ICH
SRC11	



REQ PORT LIST

PORT	DEVICE
REQ_3#	MCH_3GPLL
REQ_4#	
REQ_6#	PCIE_WLAN
REQ_7#	PCIE_WWAN
REQ_9#	
REQ_10#	
REQ_11#	
REQ_A#	SATA

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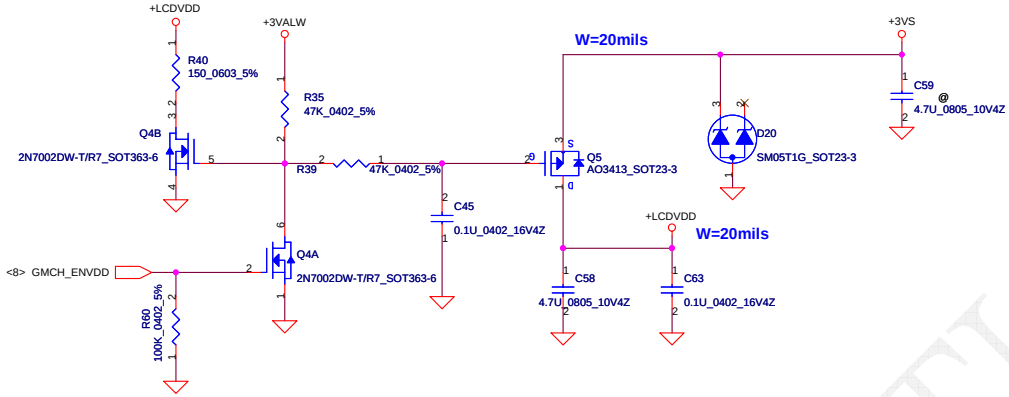
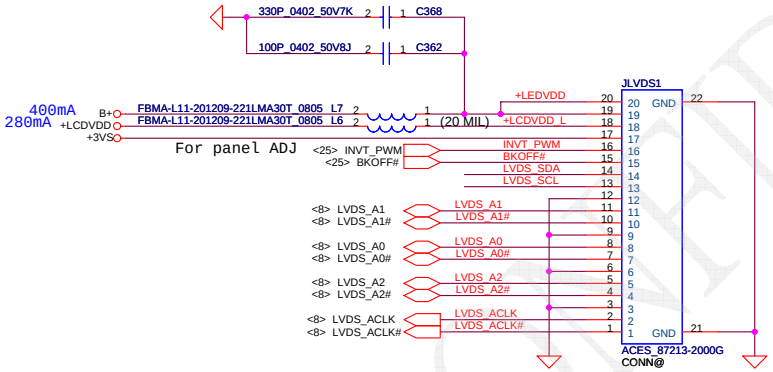
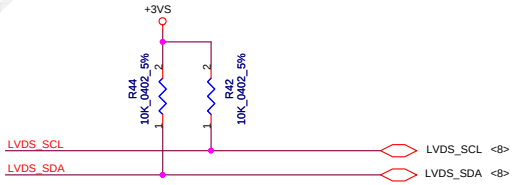
LCD POWER CIRCUIT



LCD/PANEL BD. Conn.





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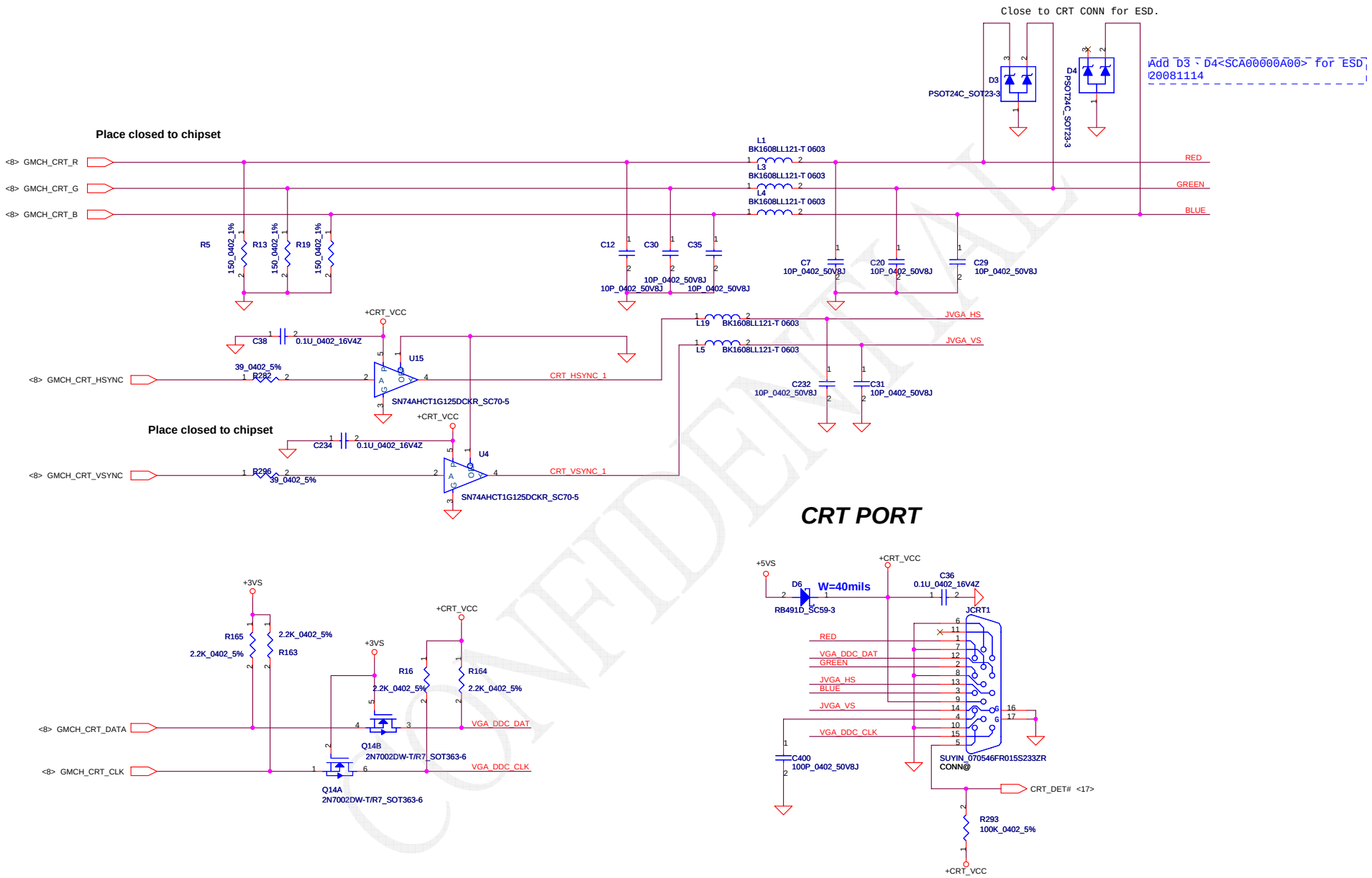

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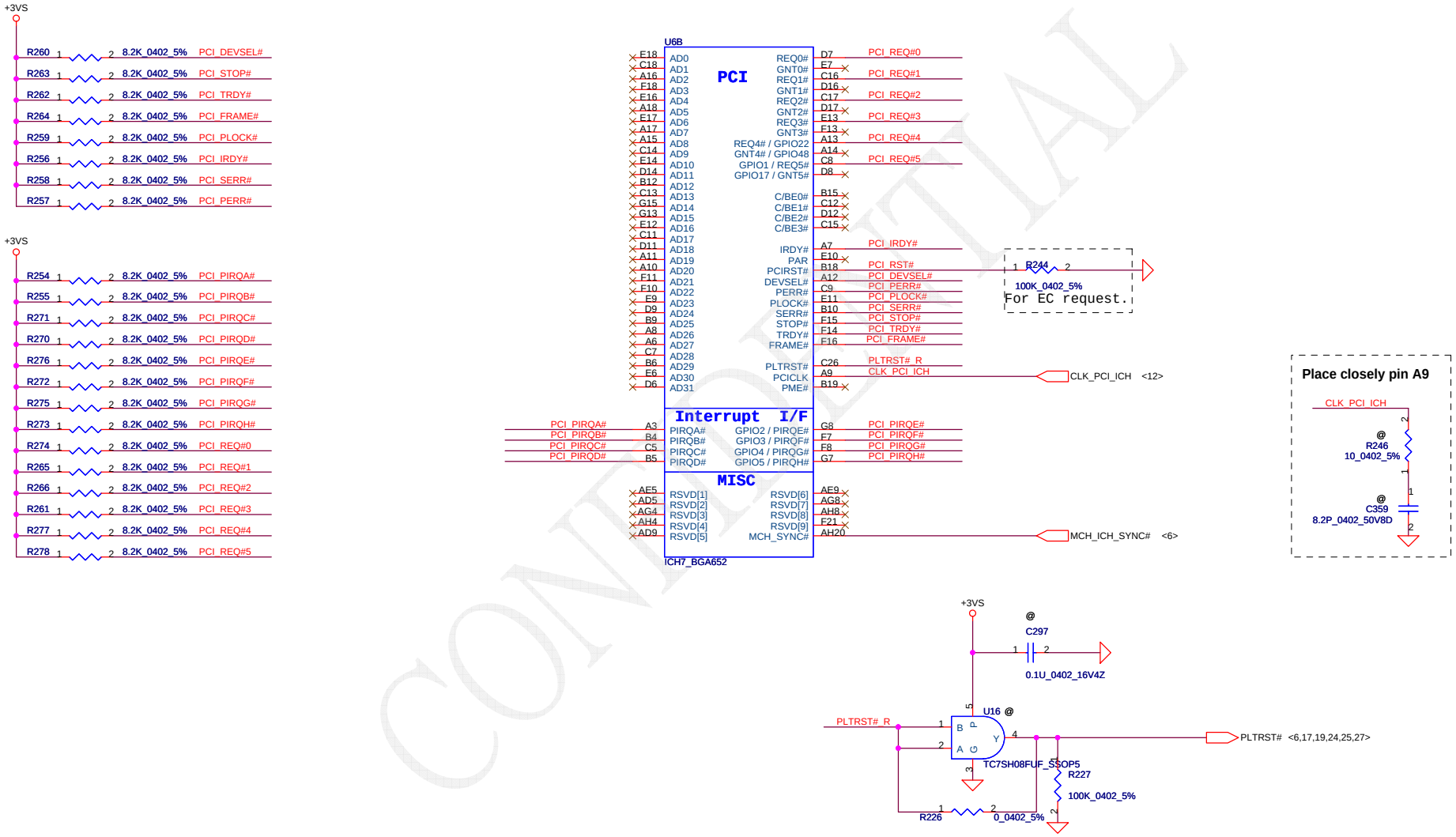

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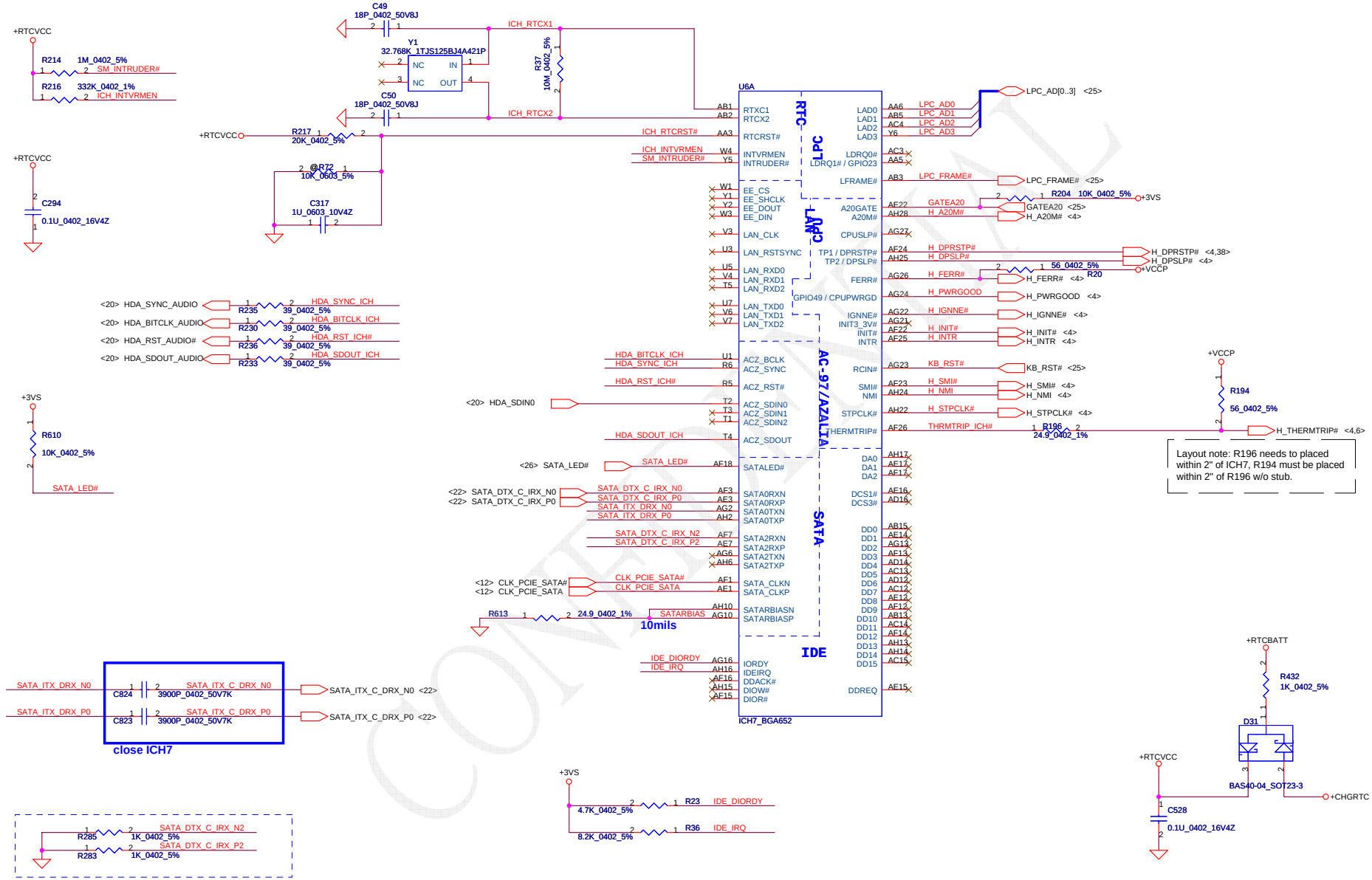

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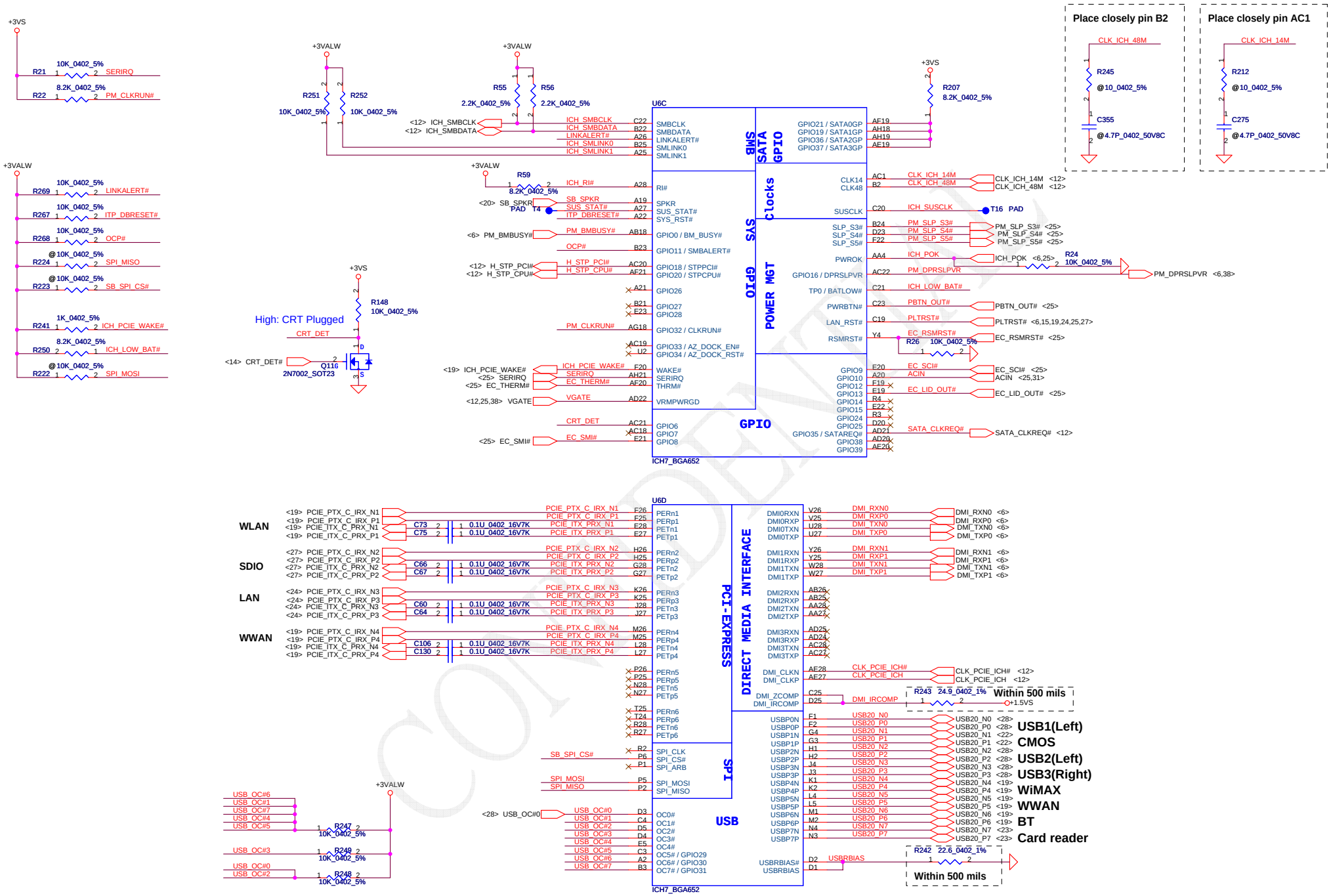

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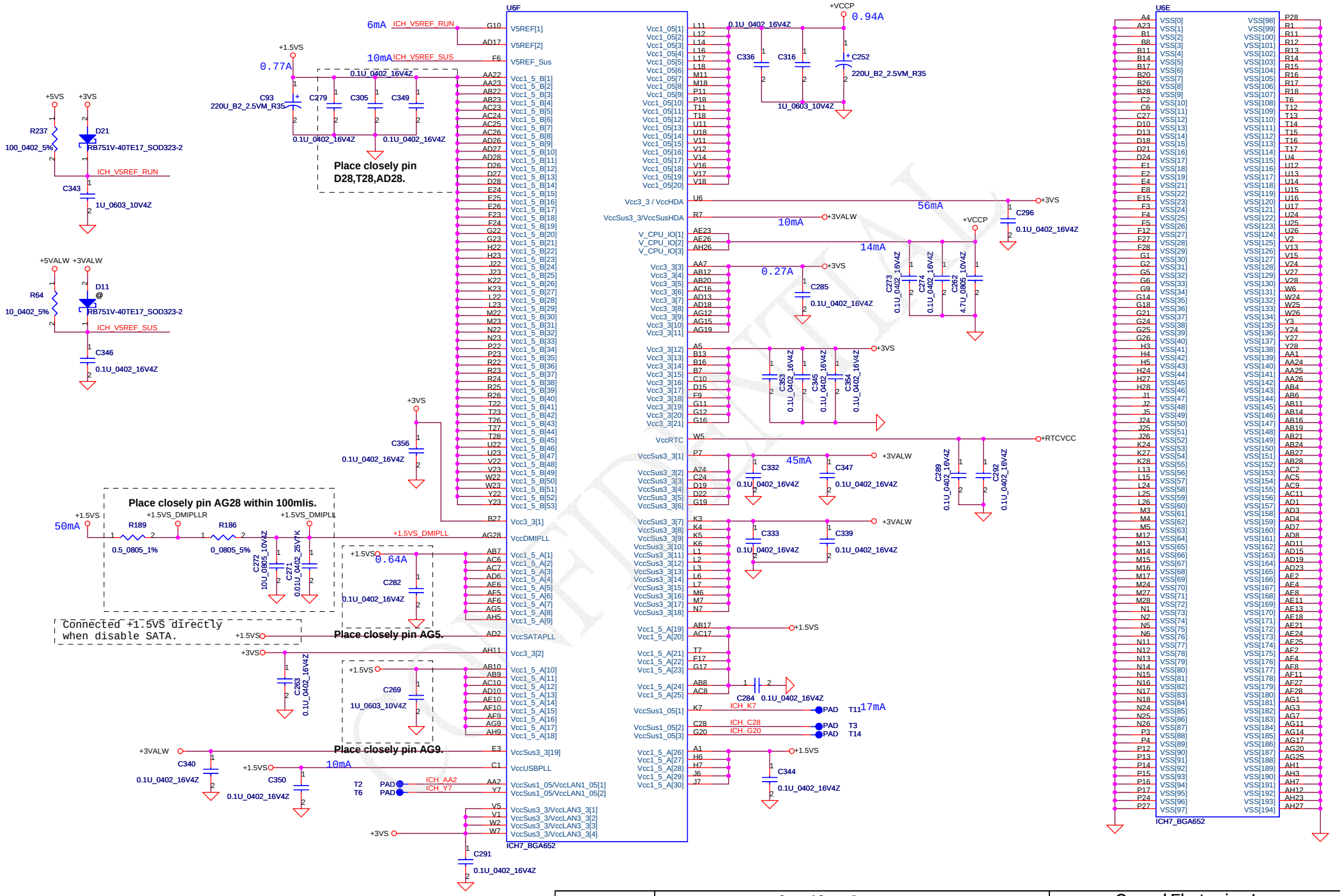

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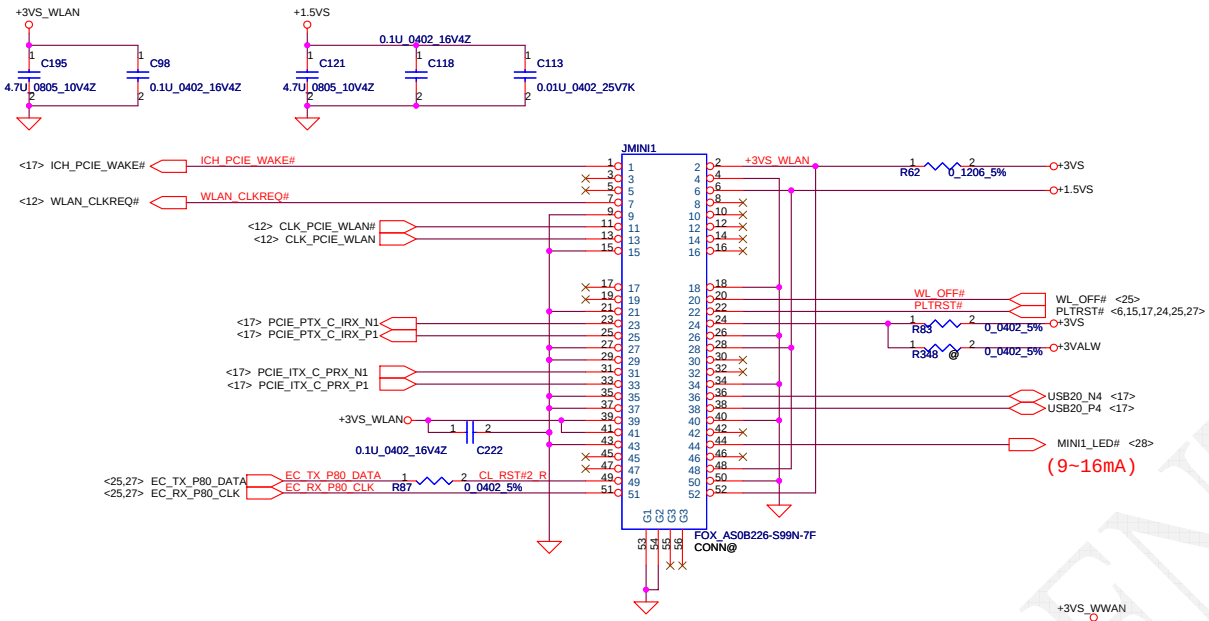
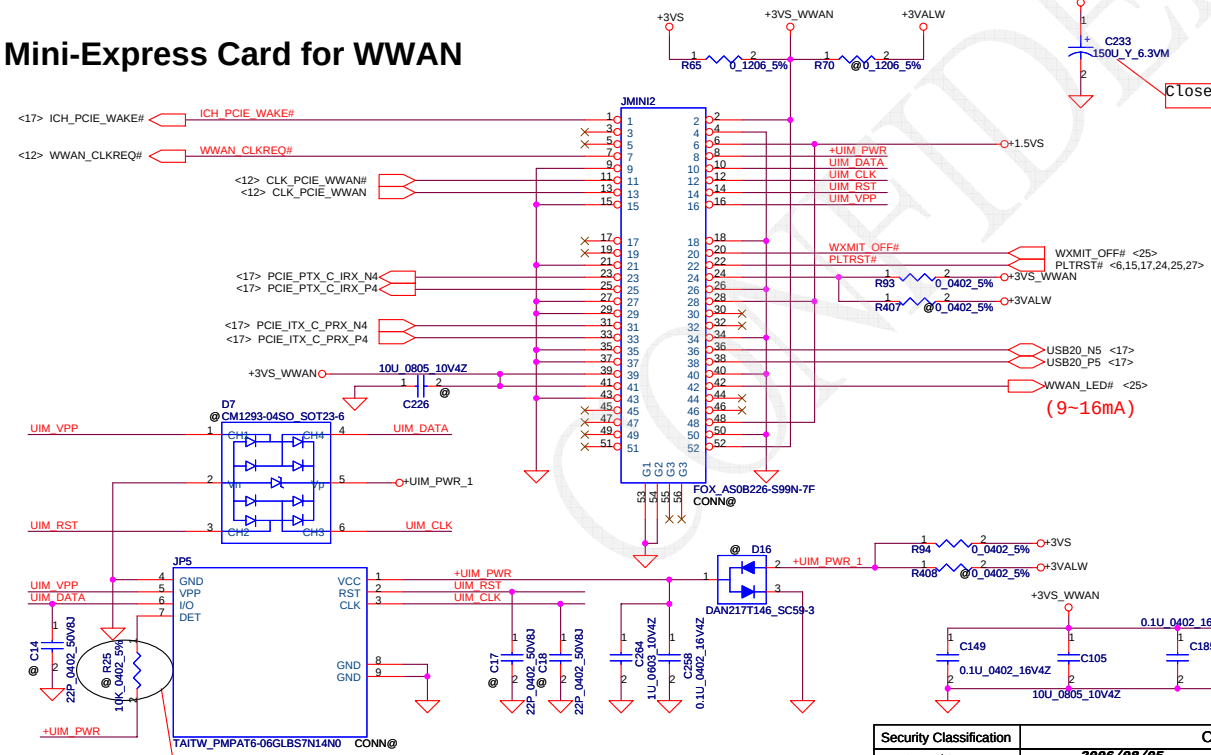
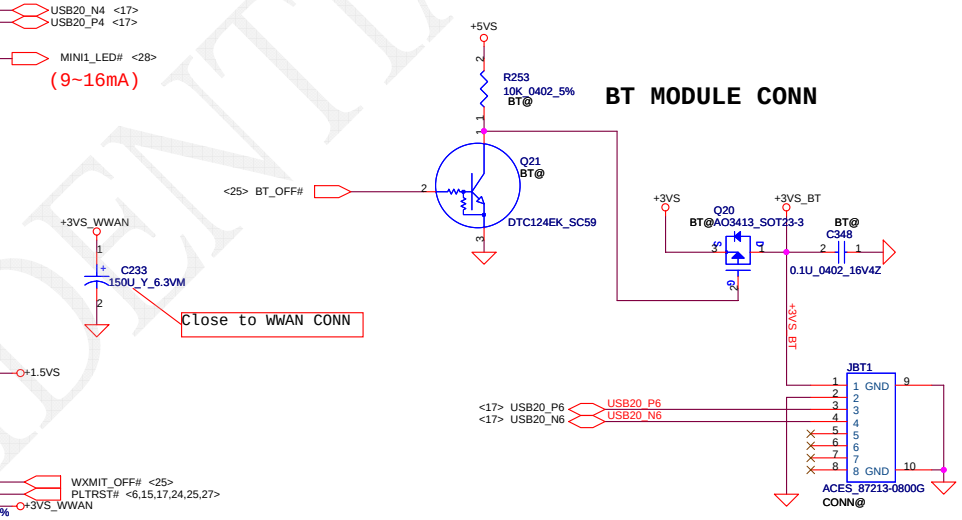
Mini-Express Card for WLAN



Mini-Express Card for WWAN



Reserve for SIM card does not meet rise time and pull-up is needed.



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				Date: Thursday, April 02, 2009 — Sheet 19 of 40

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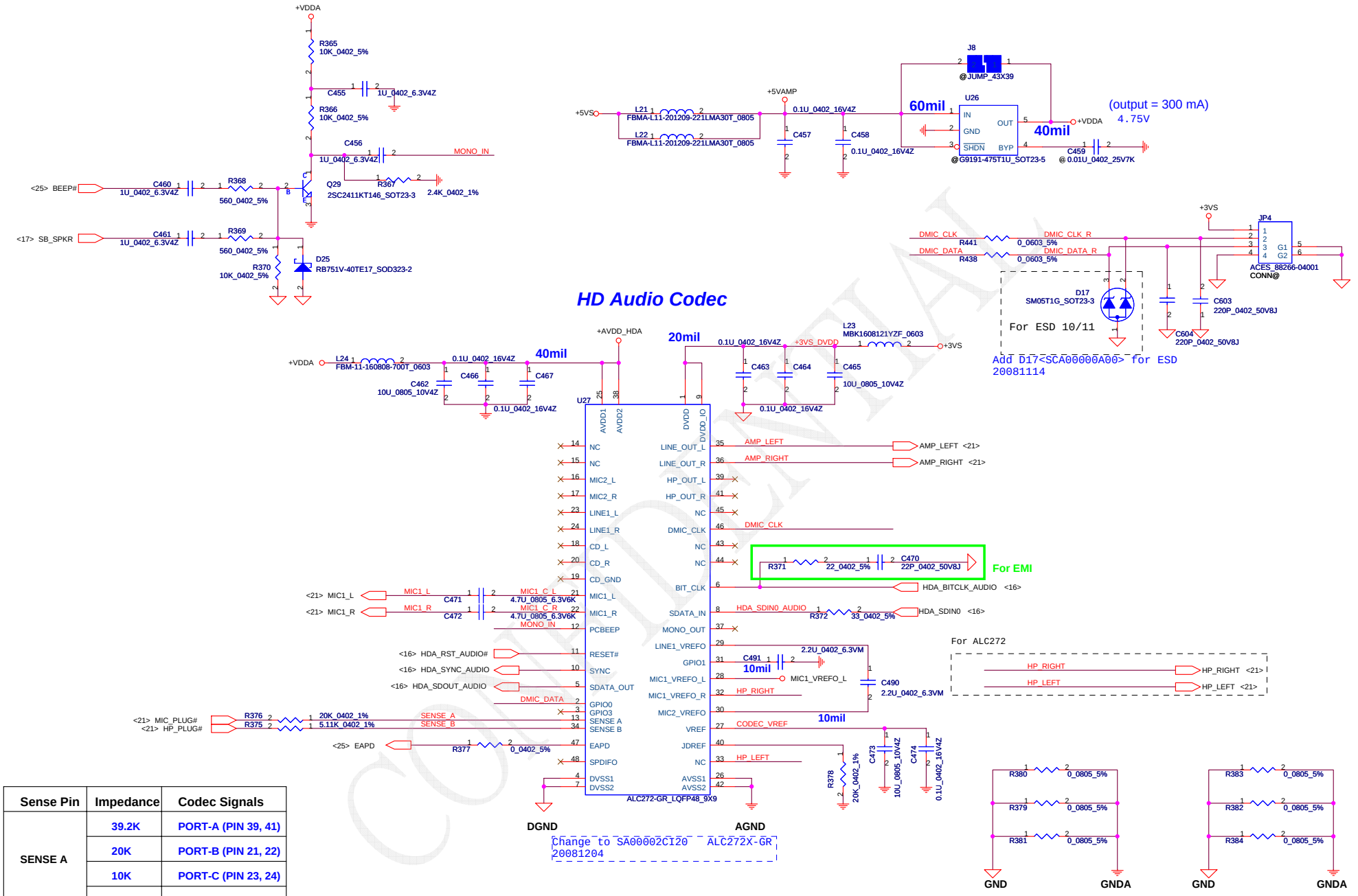

Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

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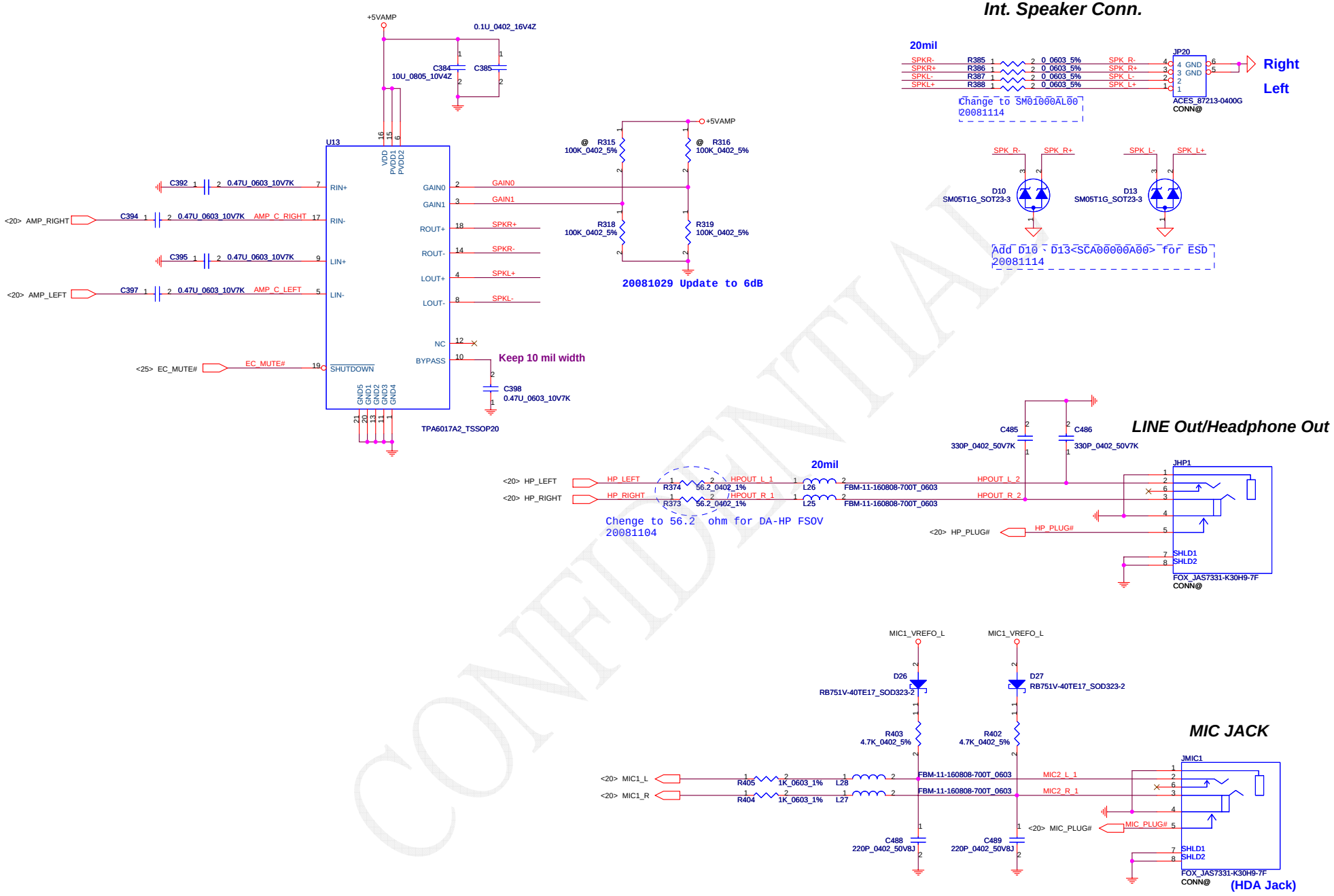

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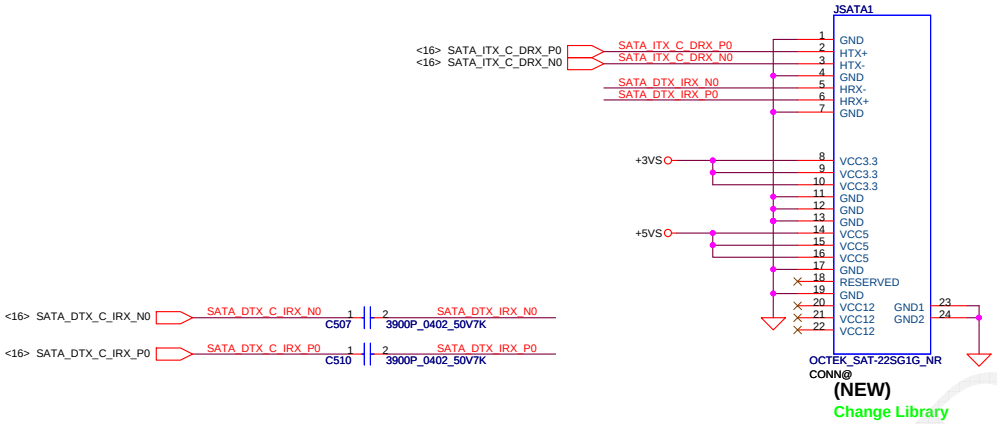
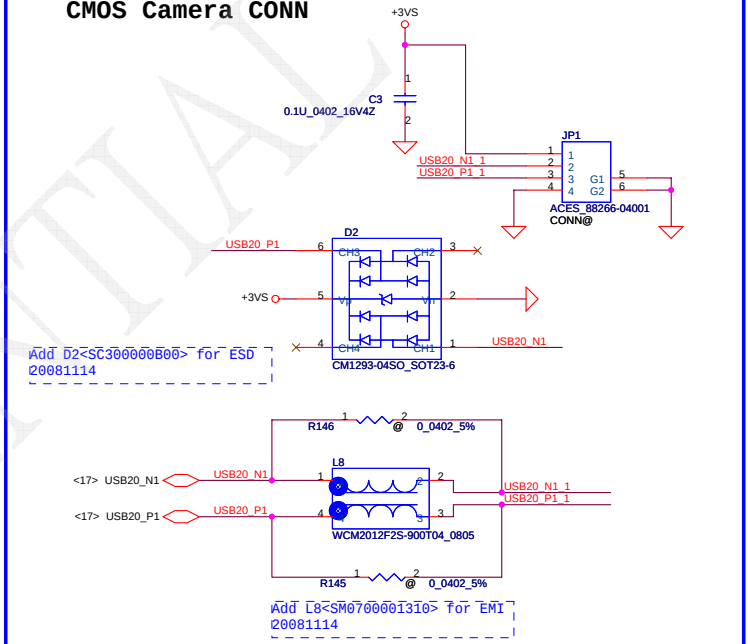
SATA HDD Conn.



(NEW)

Change Library

CMOS Camera CONN



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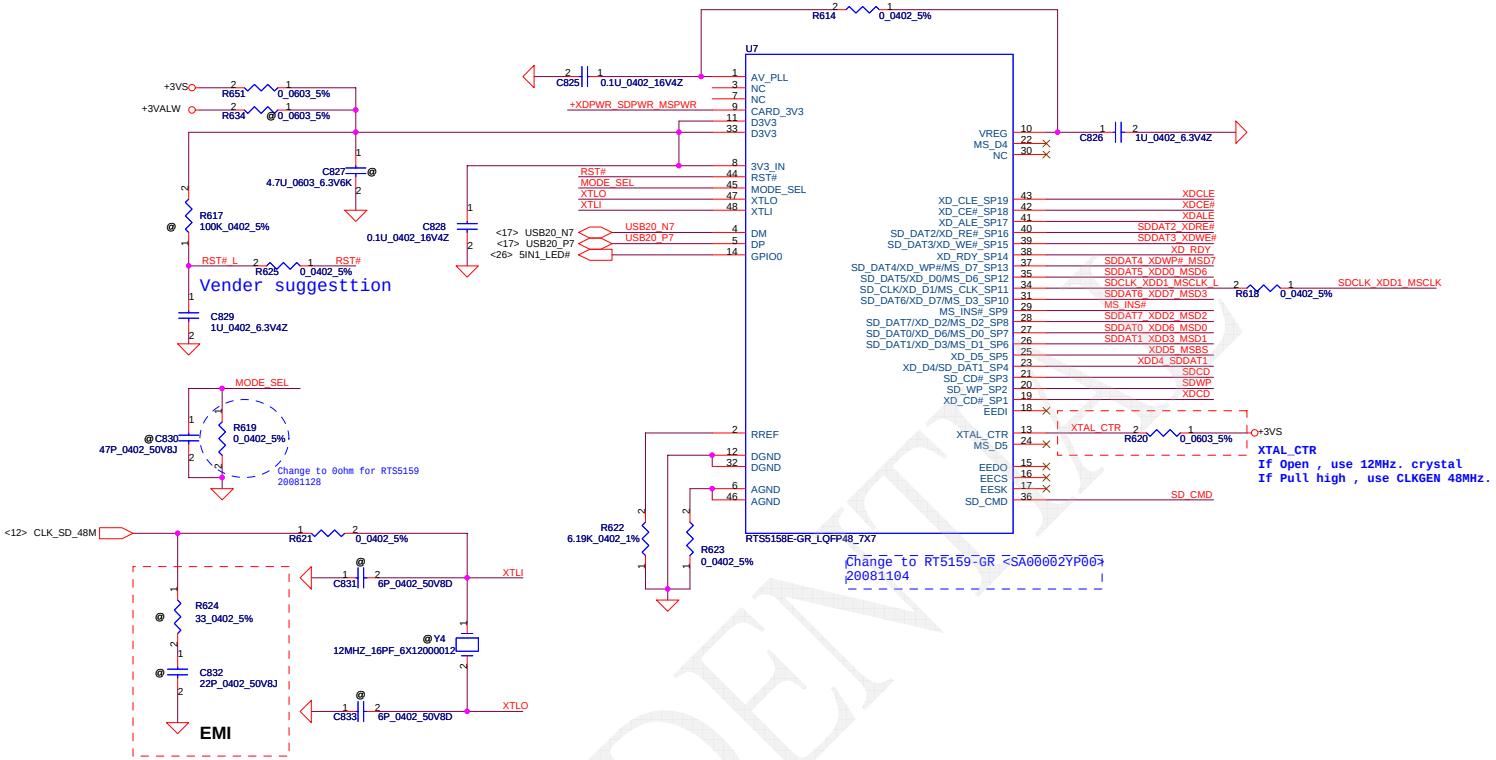

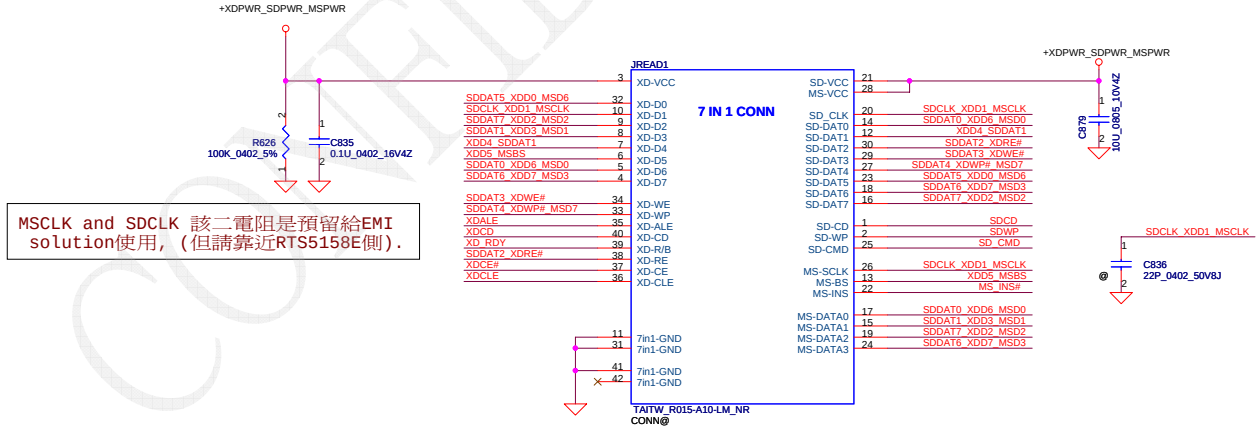

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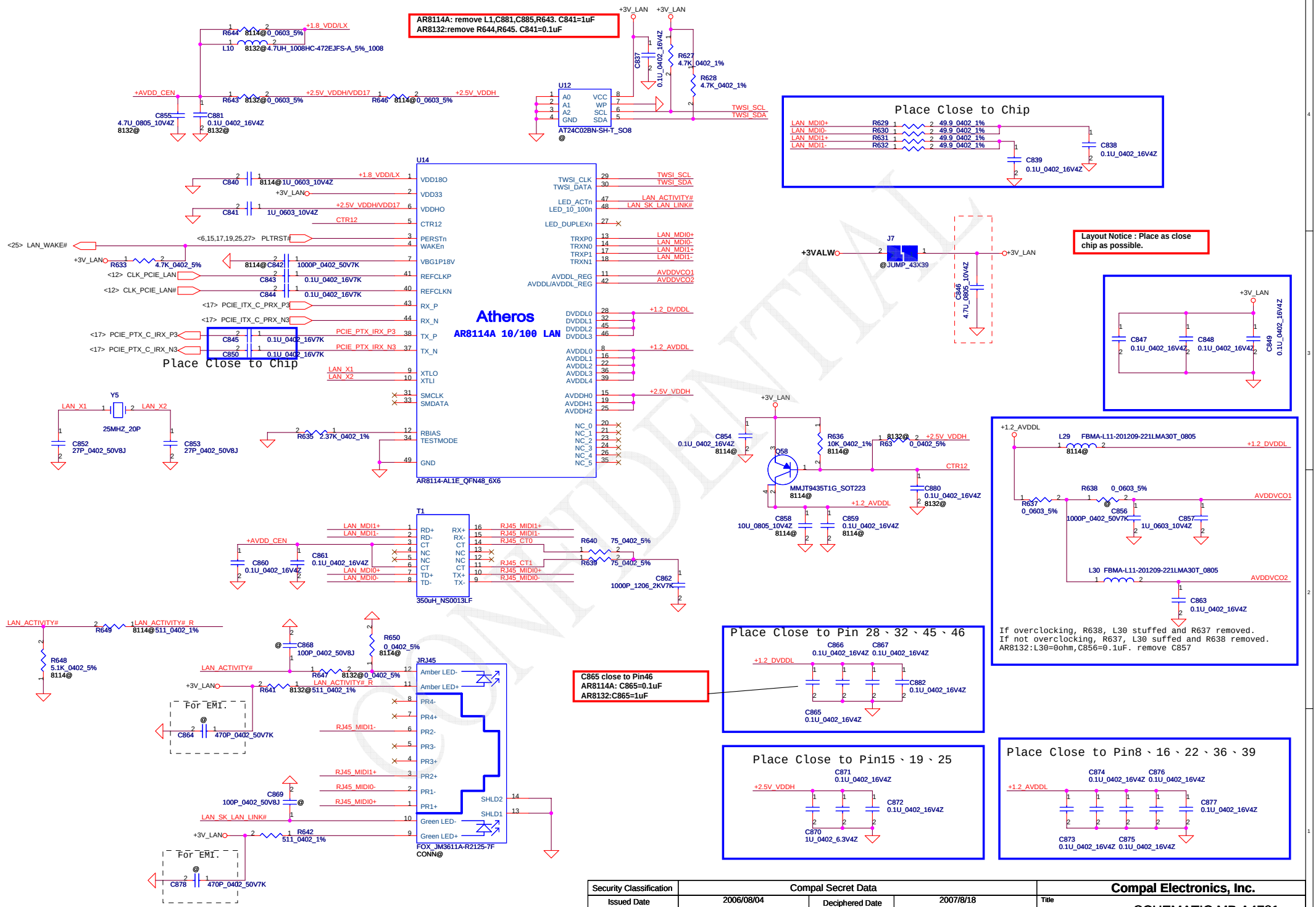

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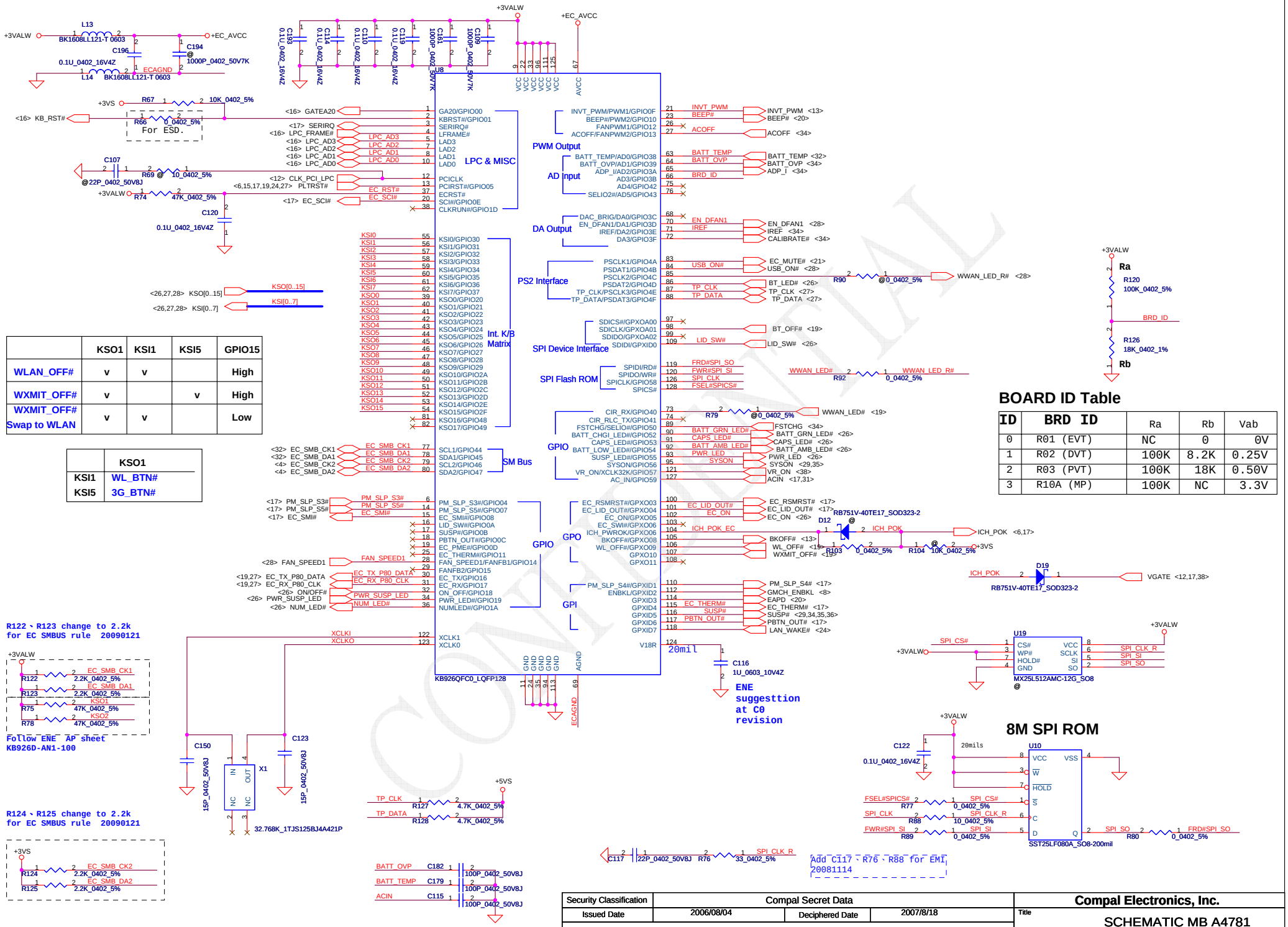

	KSO1	KSI1	KSI5	GPIO15
WLAN_OFF#	v	v		High
WXMIT_OFF#	v		v	High
WXMIT_OFF# Swap to WLAN	v	v		Low

	KSO1
KSI1	WL_BTN#
KSI5	3G_BTN#

ID	BRD ID	Ra	Rb	Vab
0	R01 (EVT)	NC	0	0V
1	R02 (DVT)	100K	8.2K	0.25V
2	R03 (PVT)	100K	18K	0.50V
3	R10A (MP)	100K	NC	3.3V

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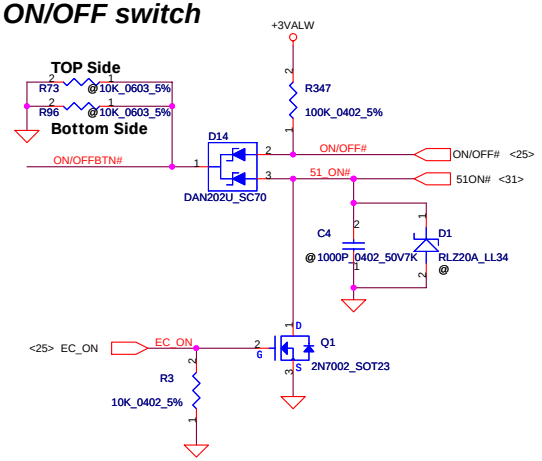
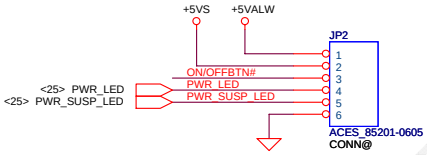
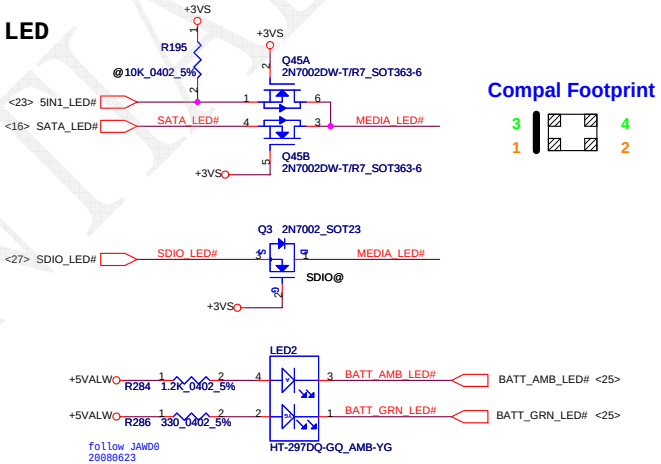
ON/OFF switch



To PWR/B Conn.

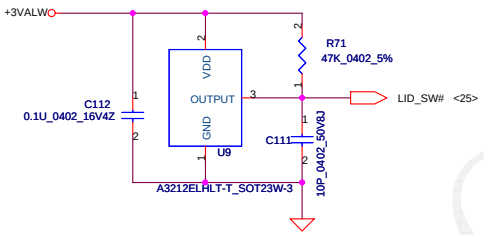


LED

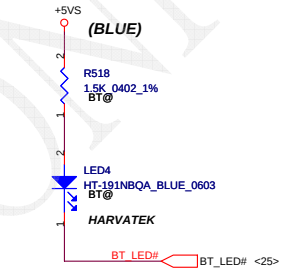


Compal Footprint

LID Switch



Bluetooth LED



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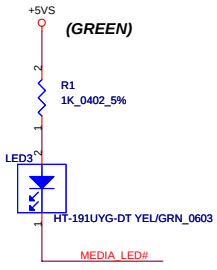

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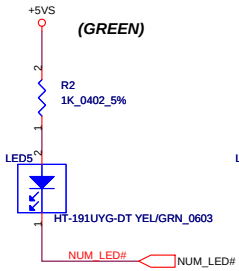
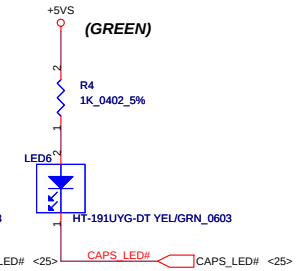
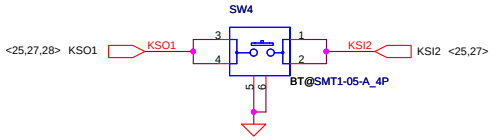


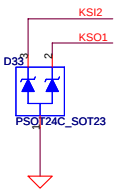
CAPS_LED



Bluetooth Button



	KSO1
KSI2	BT_BTN#



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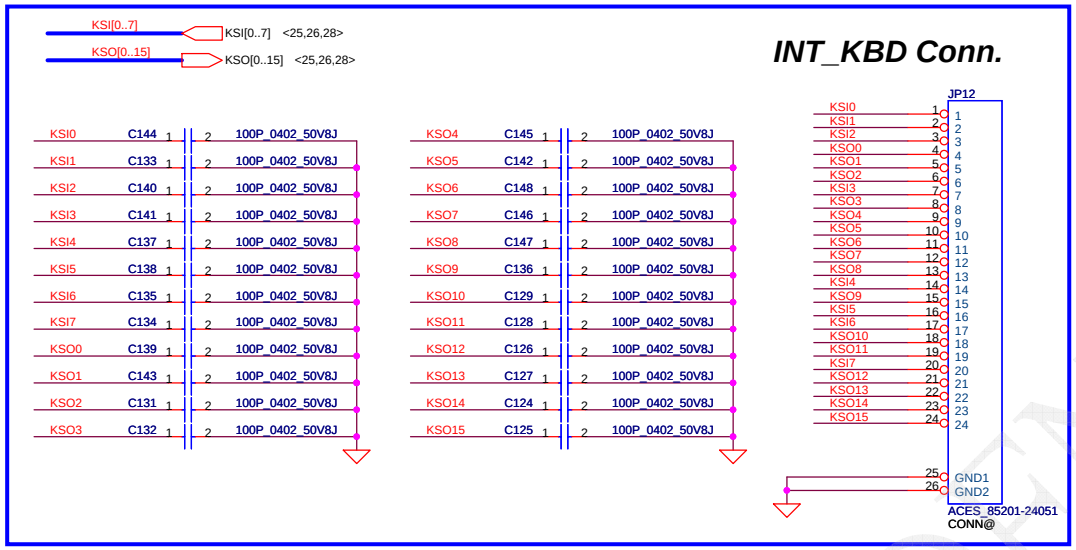

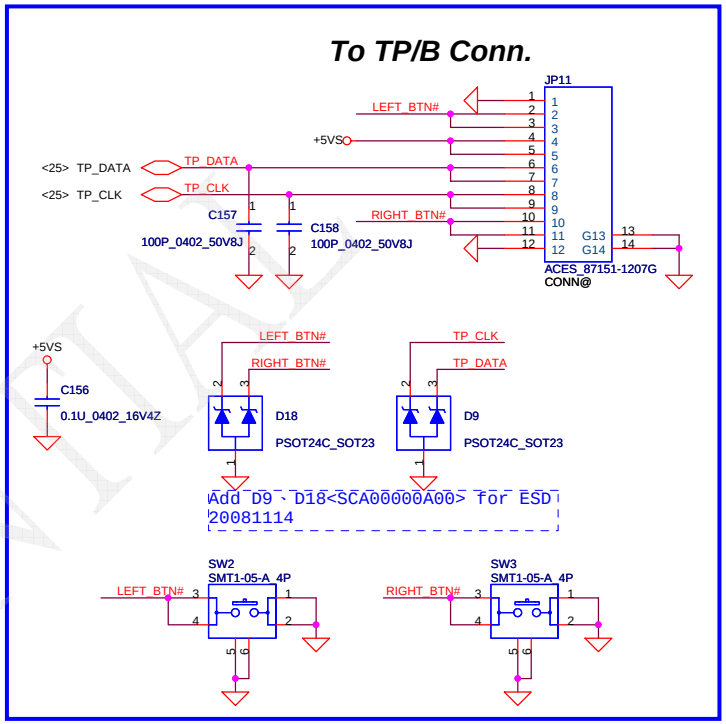

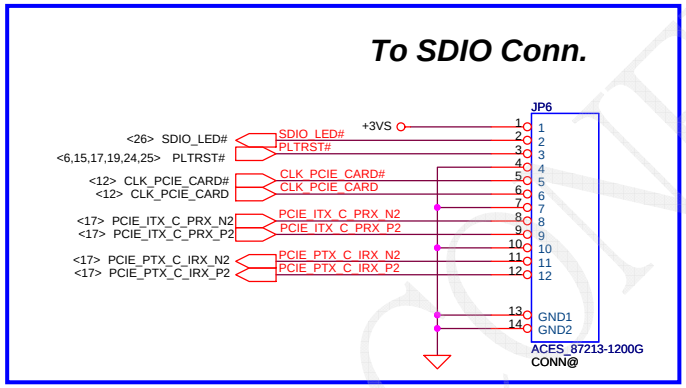

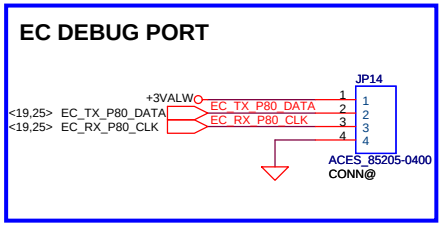

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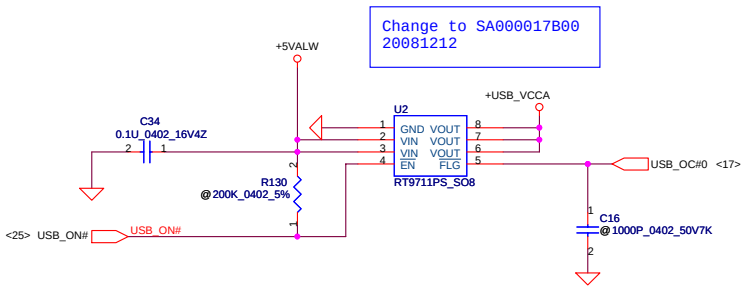
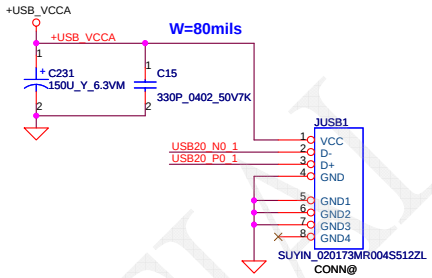
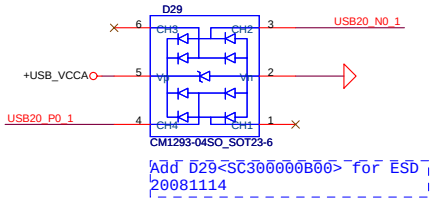
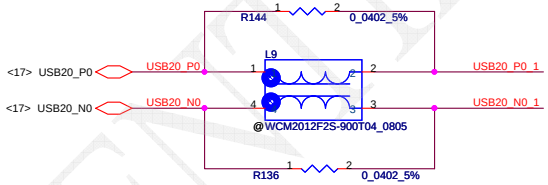


USB CONN. 1



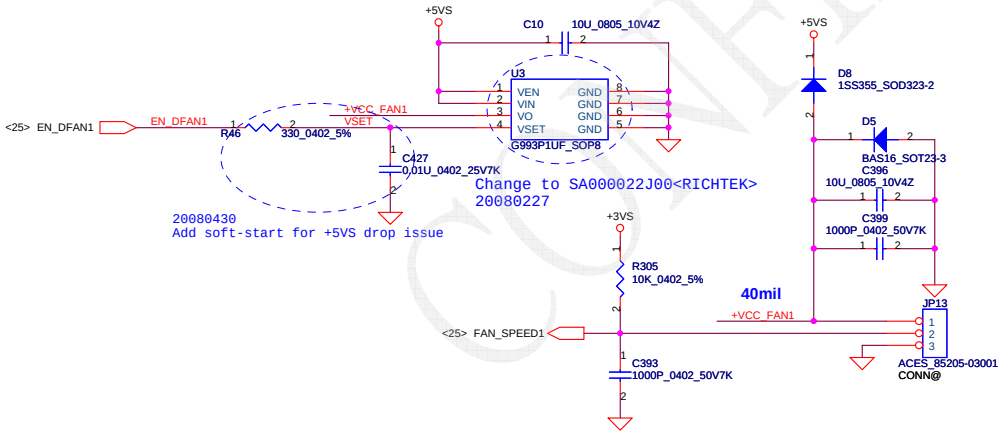


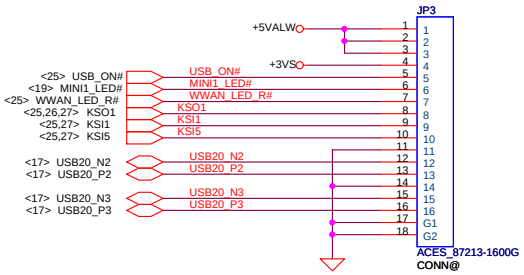


To USB/B Conn.

	KSO1
KSI1	WL_BTN#
KSI5	3G_BTN#

FAN1 Conn





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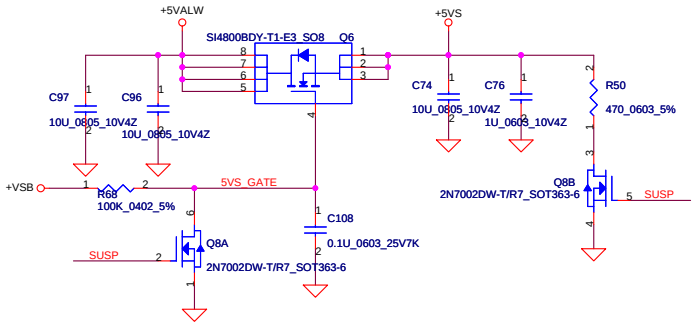
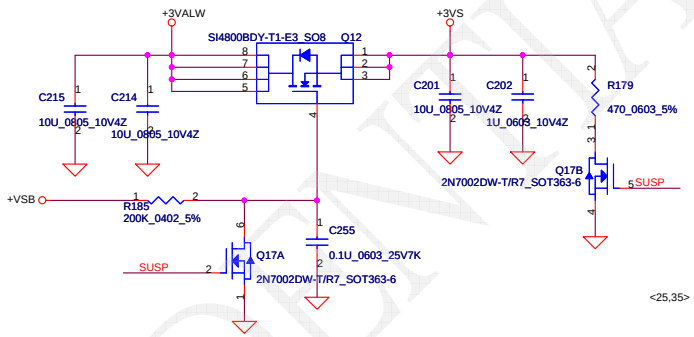
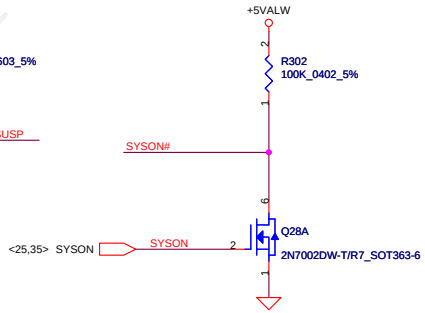
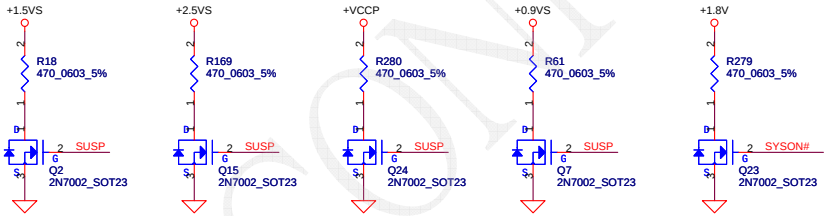
+5VALW TO +5VS

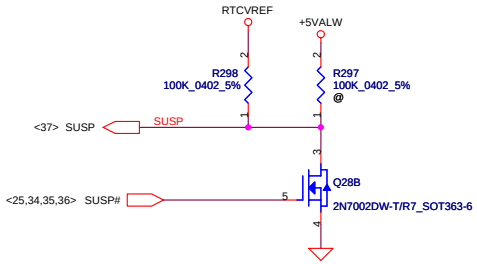


+3VALW TO +3VS









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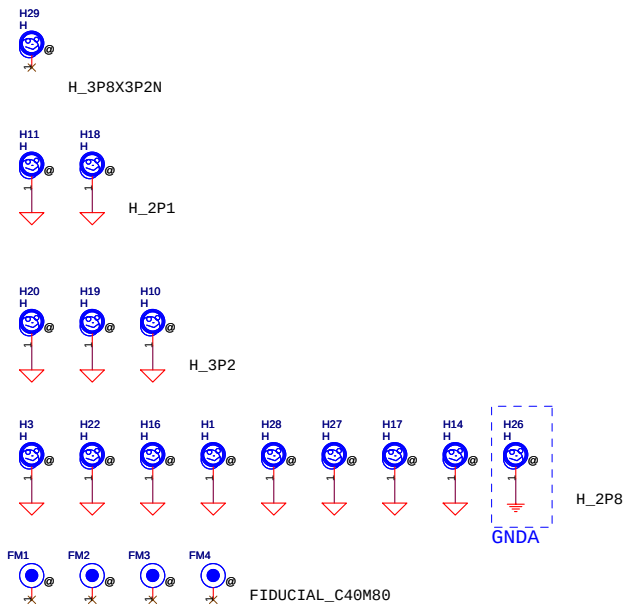

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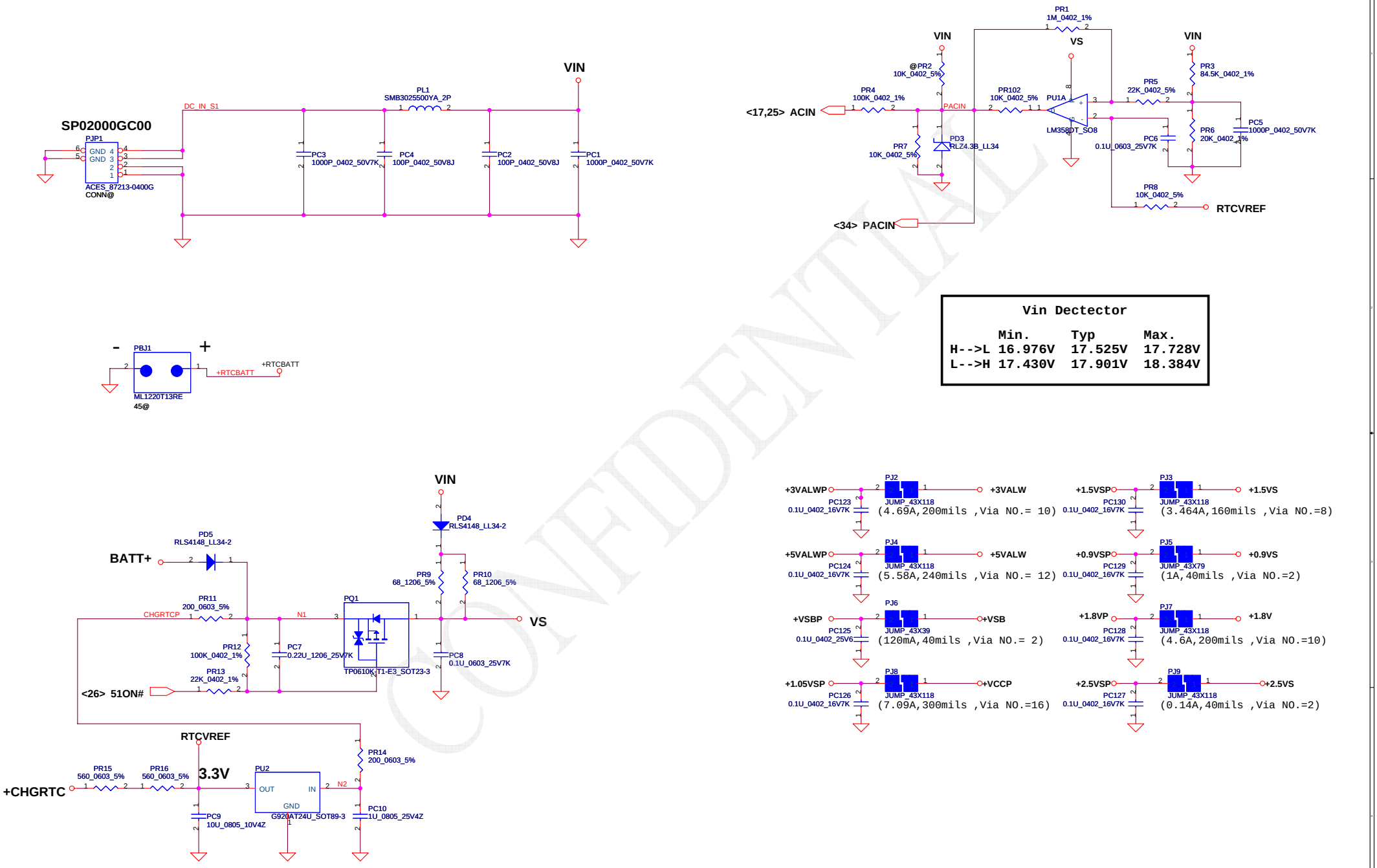

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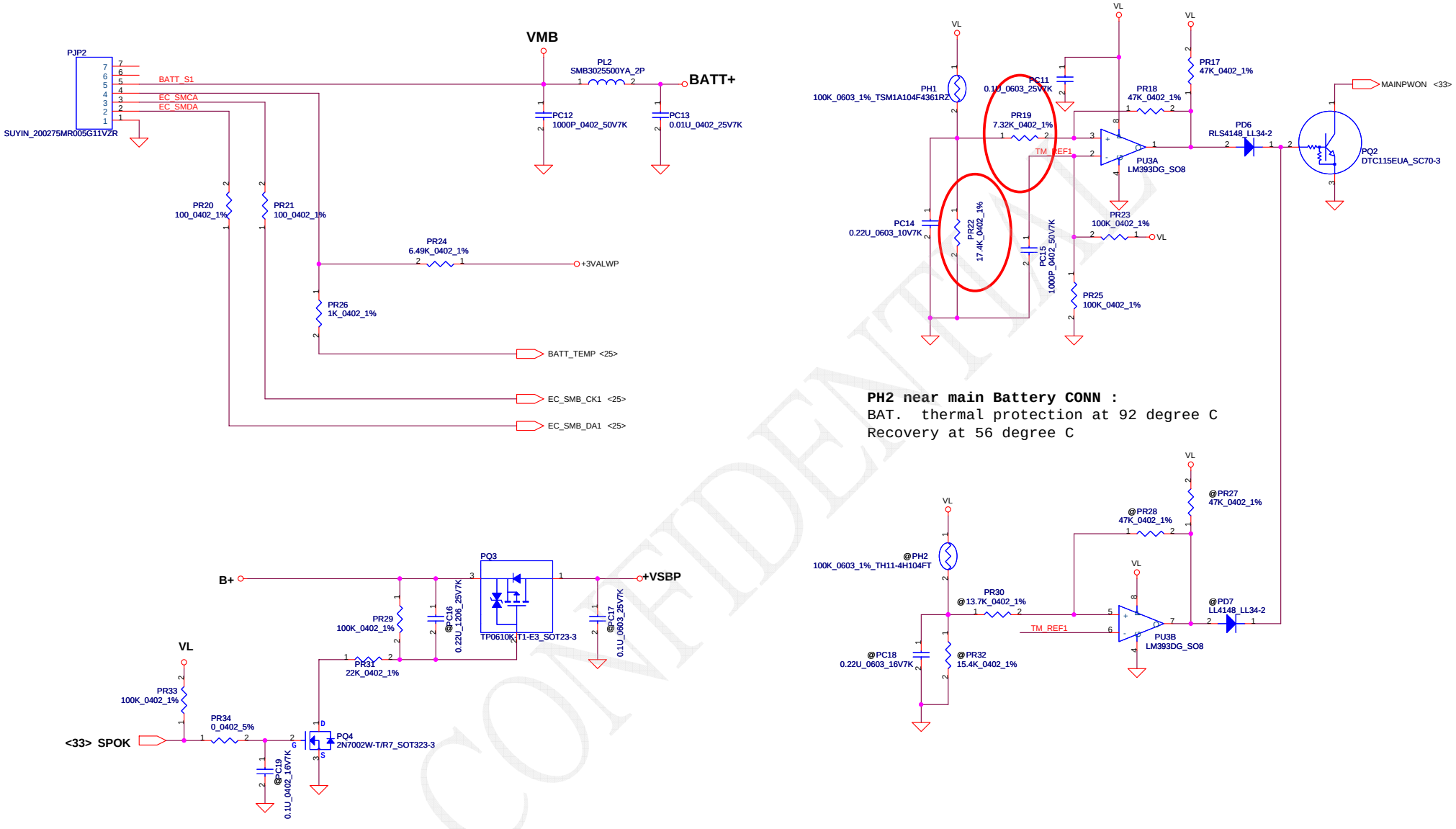
PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C



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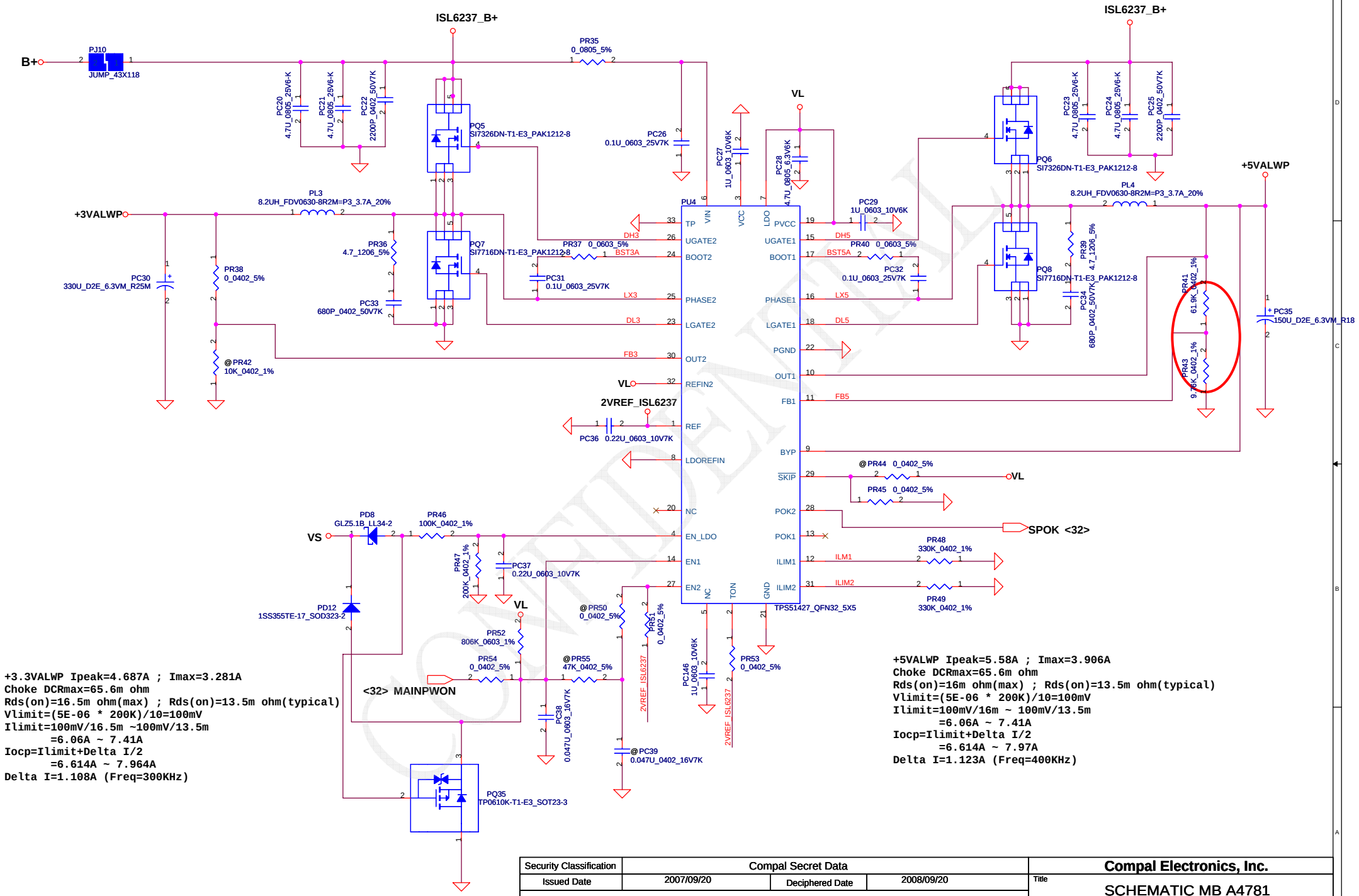

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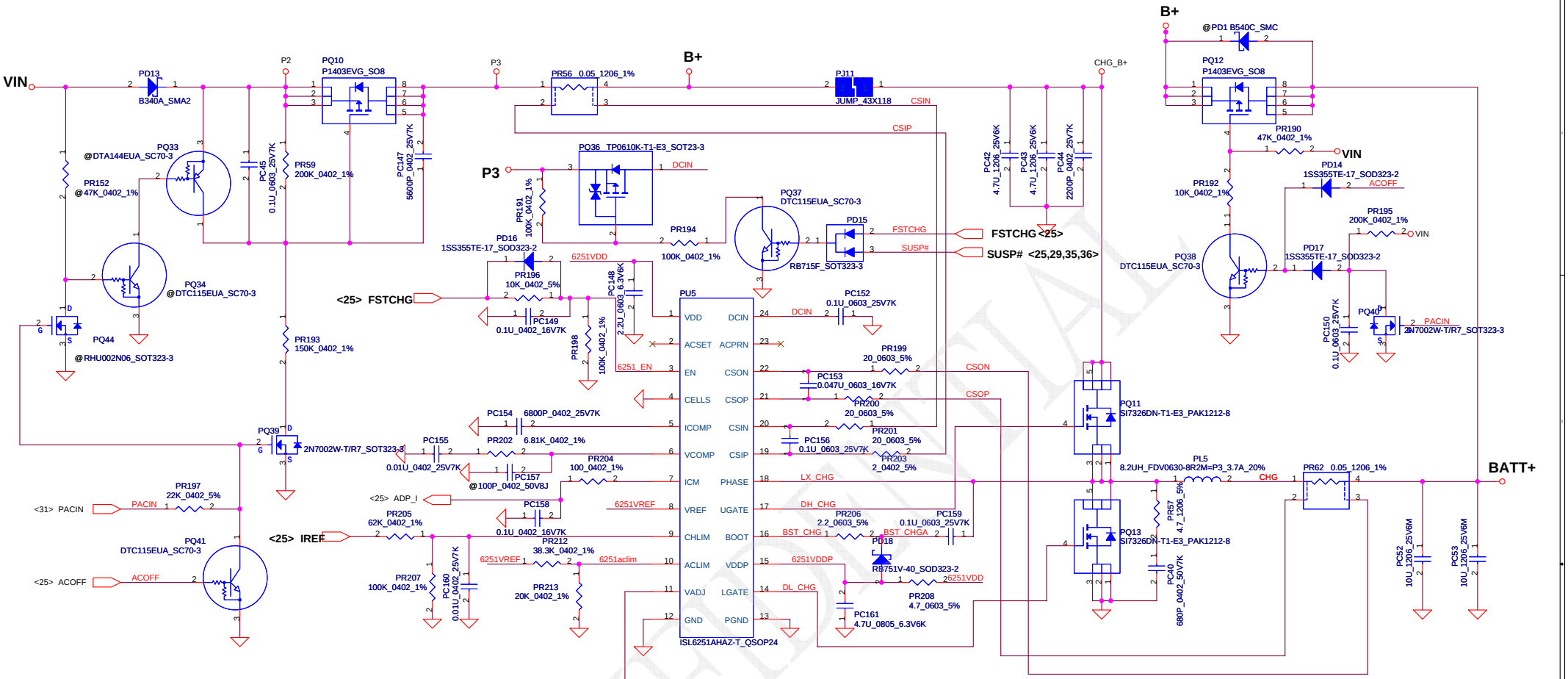

Iada=0~1.58A(30W) CP = 85%*Iada ; CP = 1.343A

CP mode
Vaclim=2.39*(20K/(20K+38.3K))=0.8199V

Iinput=(1/0.05)((0.05*Vaclm)/2.39+0.05)
where Vaclm=0.8199V, Iinput=1.343A

CC=0.3~1.76A
IREF=1.62*Icharge
IREF=0.486V~2.85V
3.24V==>2A

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

CALIBRATE#	Pre Cell
H	4.35V
L	3.99V

VADJ-->VREF-->4.41V
VADJ--->Ground--->3.39V
Vcell=(0.175*VADJ+3.99)

LI-3S :13.5V----BATT-OVP=1.5012V
BATT-OVP=0.1112*VMB
Per cell=3.5V

Charger ADJ	Calibrate#	PR211	PR220
4.2V	N/A	@	@
3.99V	L	301K	499K
4.35V	H	301K	499K

-

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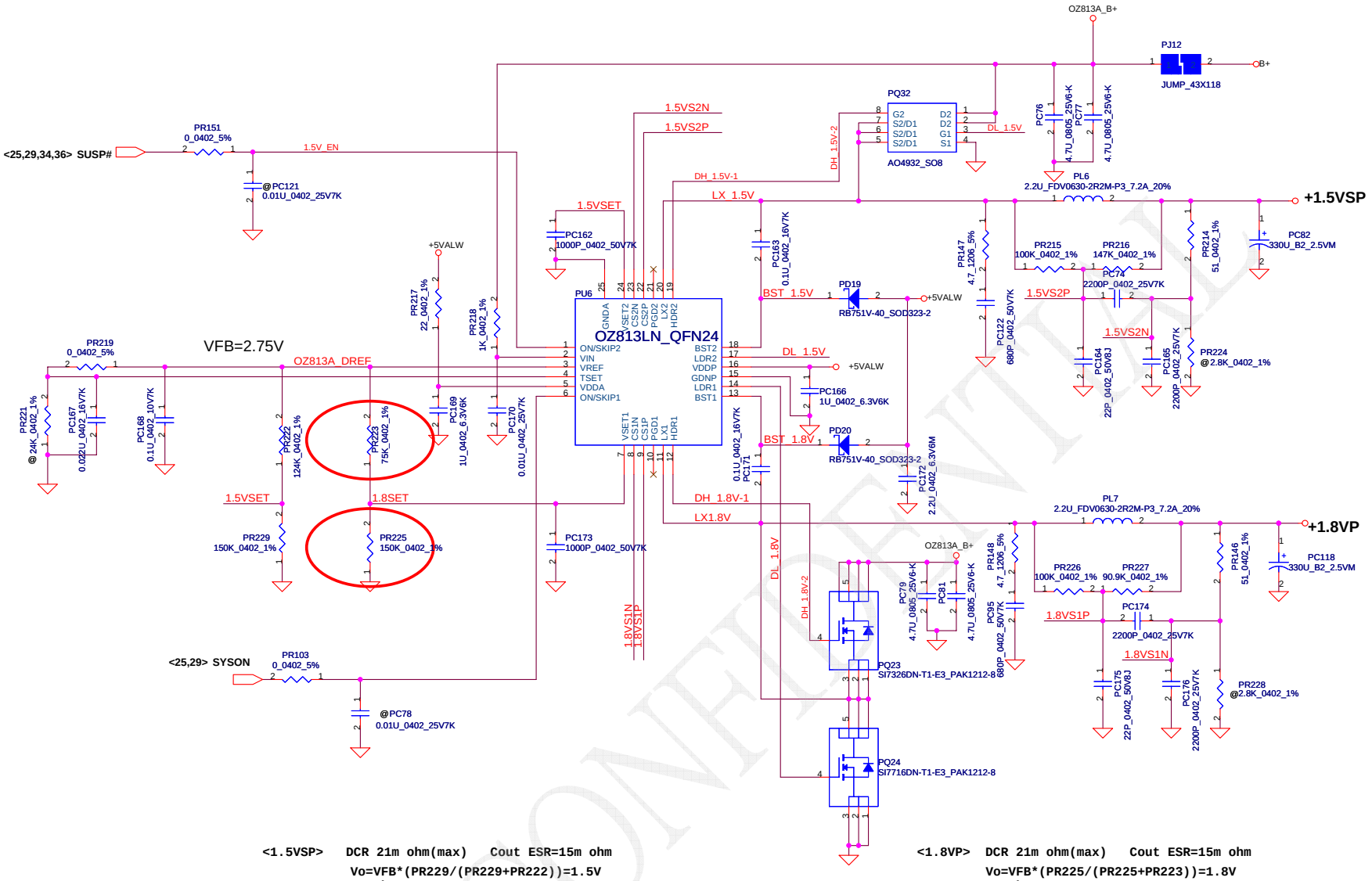

<1.5VSP> DCR 21m ohm(max) Cout ESR=15m ohm
Vo=VFB*(PR229/(PR229+PR222))=1.5V
Ipeak=3.464A, Imax=2.425A, Iocp=5A

<1.8VP> DCR 21m ohm(max) Cout ESR=15m ohm
Vo=VFB*(PR225/(PR225+PR223))=1.8V
Ipeak=4.6A, Imax=3.22A, Iocp=6A

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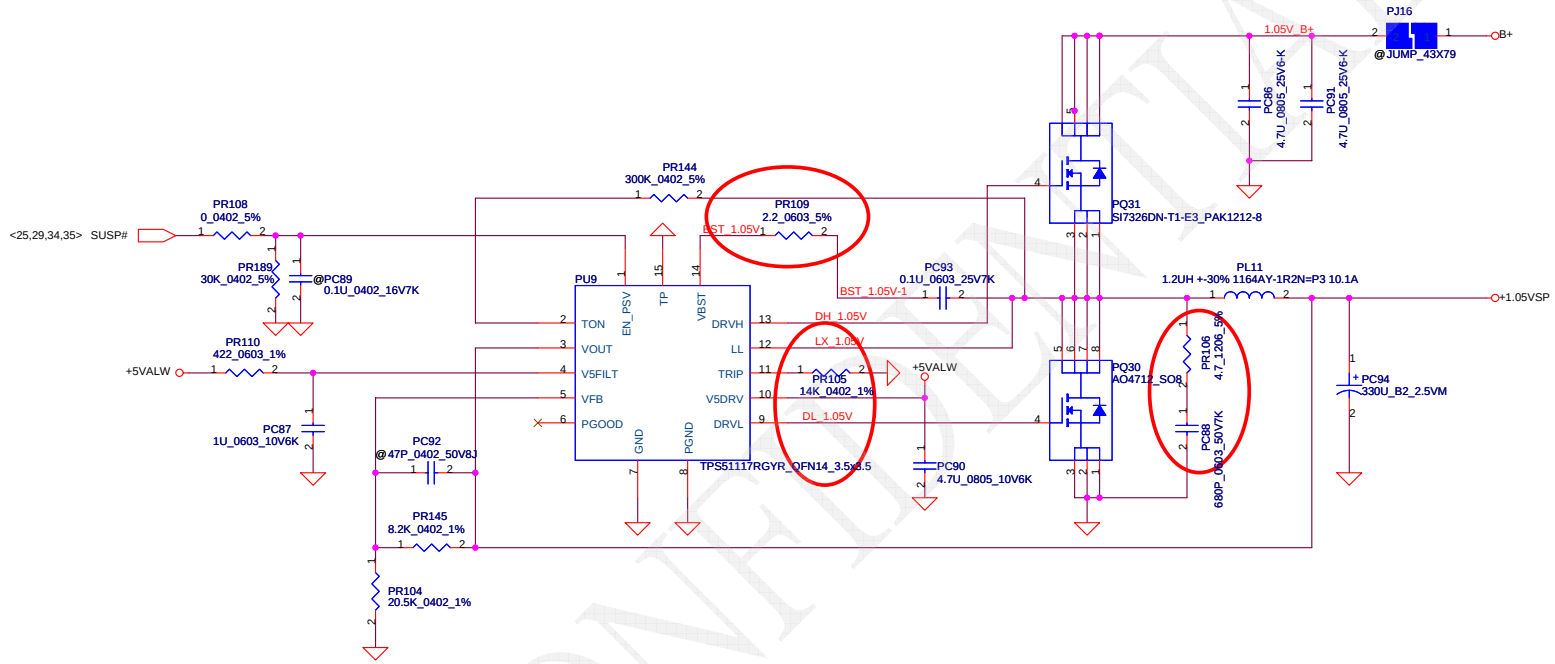

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```
<Vo=1.05V>  VFB=0.75V
Vo=VFB*(1+PR145/PR104)=0.75*(1+8.2K/20.5K)=1.05V
Fsw=261KHz


Cout ESR=15m ohm Rdson(max)=16.5m  Rdson(typical)=13.5m
Ipeak=7.09A, Imax=4.963A, Iocp=8.51A
Delta I=((19-1.05)*(1.05/19))/(1.5u*261K)=2.53A
=>1/2DeltaI=1.265A
Vtrip=Rtrip*10uA=14K*10uA=0.14V
Iocpmin=Vtrip/(Rdsonmax*1.2)+1.265
=0.14/(0.0165*1.2)+1.265=8.34A
Iocpmax=(0.14/(0.0135*1.2))+1.265A=9.91A
Iocp=8.34A~9.91A
```

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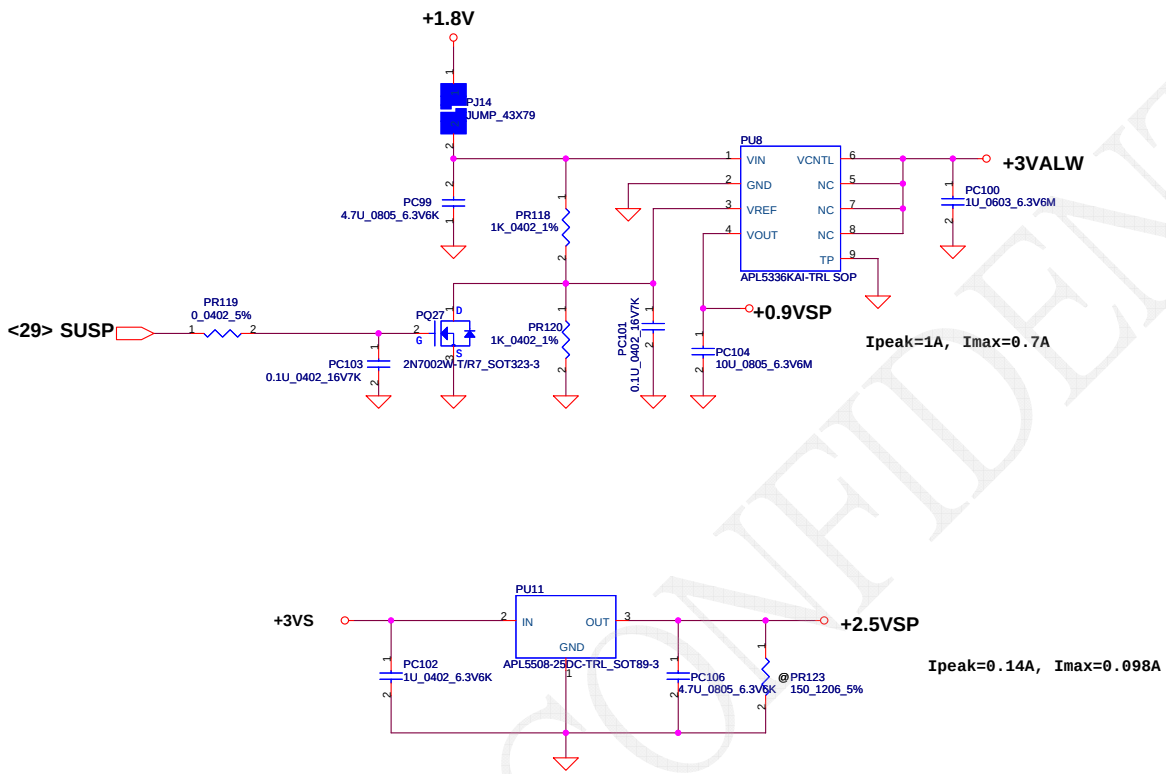

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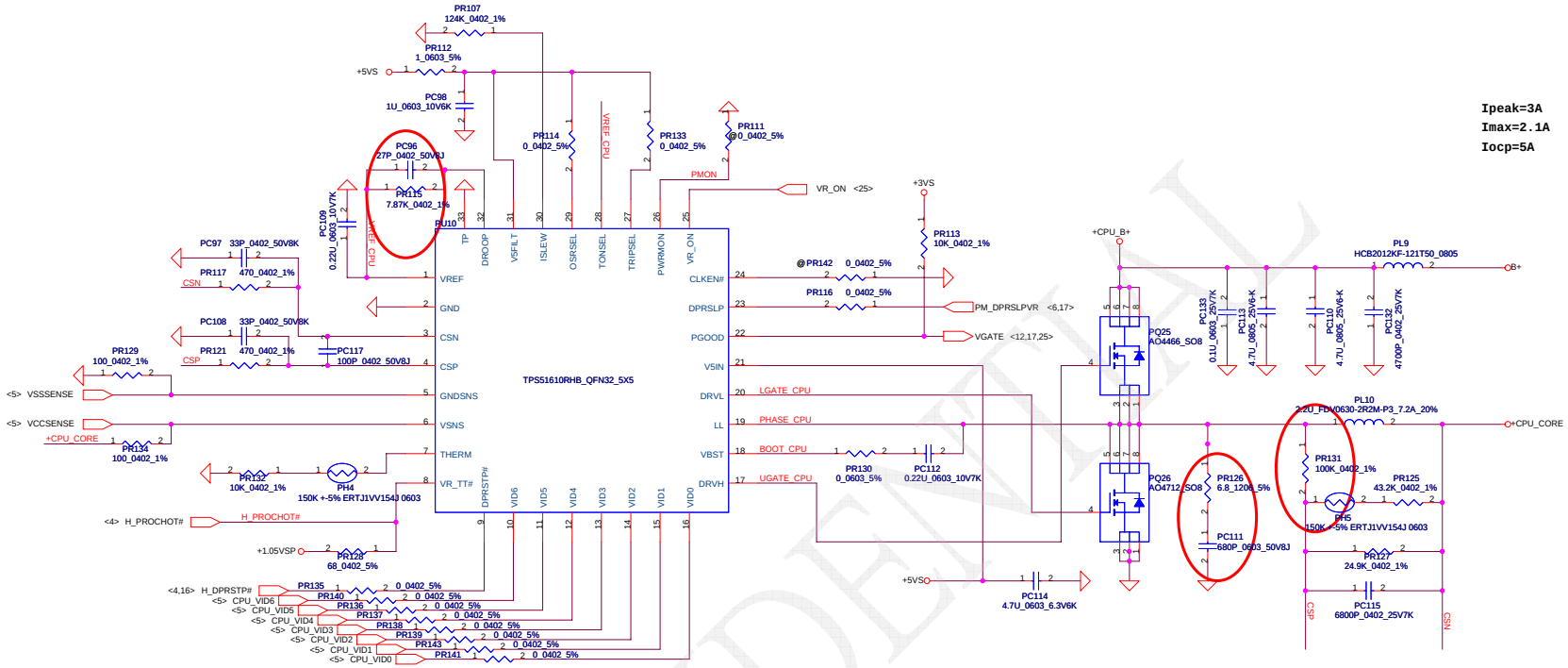

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Version change list (P.I.R. List)

for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Modify CPU_CORE VR_TT# circuit	circuit error	0.1	38	Cahnge PR128 to SD028680A80 (S RES 1/16W 68 +-5% 0402)	08/10/27	DVT
2	Diode modify	BOM error	0.1	31	Cahnge PD3 to SC4LZ43B0T4 (S ZEN DIO RLZ4.3B (LL-34))	08/10/27	DVT
3	Diode modify	BOM error	0.1	31	Cahnge PD4 to SC11N414880 (S DIO RLS4148 LL34)	08/10/27	DVT
4	Diode modify	BOM error	0.1	31	Cahnge PD5 to SC11N414880 (S DIO RLS4148 LL34)	08/10/27	DVT
5	Diode modify	BOM error	0.1	32	Cahnge PD6 to SC11N414880 (S DIO RLS4148 LL34)	08/10/27	DVT
6	Add 3/5V,charger,1.8/1.5V snubber	For ESD solution	0.1	33	Add PR36 PR39 PR57 PR147 PR148 to SD001470B80 (S RES 1/4W 4.7 +-5% 1206) Add PC33 PC34 PC40 PC122 PC95 to SE074681K80 (S CER CAP 680P 50V K X7R 0402)	08/10/27	DVT
7	Add CPU snubber	For ESD solution	0.1	33	Add PR126 to SD011680B80 (S RES 1/4W 6.8 +-5% 1206) Add PC111 to SE024681J80 (S CER CAP 680P 50V J NPO 0603)	08/10/27	DVT
8	Add CPU_CORE input capacitance	For ESD solution	0.1	38	Add PC133 SE042104K80 (S CER CAP .1U 25V K X7R 0603) Add PC132 SE074222K80 (S CER CAP 2200P 50V K X7R 0402)	08/10/27	DVT
9	Add CPU_CORE input capacitance	For ESD solution	0.1	31	Add PC123 PC124 PC126 PC127 PC128 PC129 PC130 to SE076104K80 (S CER CAP .1U 16V K X7R 0402) Add PC125 to SE072104K80 (S CER CAP 0.1U 25V K Y5V 0402)	08/10/27	DVT
10	Modify 1.05V LMOS	cost down	0.1	31	change PQ30 to SB00000AJ00 (S TR AO4712 1N SO8)	08/10/27	DVT
11	Modify 1.05V choke	cost down	0.1	31	change PL11 to SH00000FQ00 (S COIL 1.2UH +-30% 1164AY-1R2N=P3 10.1A)	08/10/27	DVT
12	Modify charger input capacitance size	BOM error	0.1	31	change PC42 PC43 to SE142475K80 (S CER CAP 4.7U 25V K X5R 1206 H1.6)	08/10/29	DVT
13	Modify charger VADJ circuit	circuit error					
14	Modify DIODE BOM (remove ROHN)	BOM error					
15	Modify ACIN circuit	EVT issue solution	0.1	31	change PR4 SD02800008 to SD034100380(100K)	08/11/13	DVT
16	Modify 3/5V circuit	Modify 5V voltage for HW request	0.1	33	change PR43 to SD034976180 (S RES 1/16W 9.76K +-1% 0402) add PR41 SD034619280(S RES 1/16W 61.9K +-1% 0402)	08/12/26	PVT
17	Modify 1.8Vcircuit	Modify 1.8V voltage for HW request	0.1	35	change PR223 to SD034750280 (S RES 1/16W 75K +-1% 0402) change PR225 to SD034150380 S RES 1/16W 150K +-1% 0402)	08/12/26	PVT
18	Modify 1.05V circuit	add snubber for SED 3G solution	0.1	36	add PC88 SE025681K80 (S CER CAP 680P 50V K X7R 0603) add PR106 SD001470B80 (S RES 1/4W 4.7 +-5% 1206)	08/12/26	PVT
19	Modify 1.05V circuit	add boost for 1.05v issue	0.1	36	change PR109 to SD013220B80 (S RES 1/10W 2.2 +-5% 0603)	08/12/26	PVT
20							
21							
22							
23							

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A-TEST Change

<8/25>
1. Update Power SCH
<8/26>
1. Update Power SCH
2. Change
   D7 SC300000D00 to SC300000O00
3.Change
   C49、C50 SE071180K80 to SE071180J80
<8/27>
1. Updata Power SCH
2. Modify
   RJ45 temp footprint FOX_JM3611A-R4122-7F_12P-T
<8/28>
1. Updata Power SCH
<9/1>
1. Updata Screw
<9/5>
1. SWAP USB20_1 Signal.
<9/10>
1. Remove Mini card pin55、pin56 的GND。
2. Change JREAD1.42、H26 to GNDA。
<9/12>
1. Swap 3G ESD pin neme。
<9/15>
1. Update Audio Jack footprint
2. Chcnge R641、R642 300ohm to 511ohm for Arthros。
3. Update L footprint。
<9/16>
1. Update POWER SCH.
<9/17>
1. Update POWER SCH.
2. ADD R380、R383 for ESD.
<9/18>
1. Update ATHEROS 10/100 LAN <AR8132/AR8114>
<9/24>
1. Change C870 0.1u to 1u.
<9/26>
1. R88 change to 0ohm.

Pre PVT-TEST Change

<10/21>
1.Remove C389 for Audio can't detect issue on page 16
2.Add KSO1/KSO2 PU +3VALW on page25
3.Add R205 for schematic mistake on page 04
4.Change EC RST to PLTRST on page 25
5.Add J8 to cost down Audio LDO on page 20
6.Add R72 to reserve +3VALW for 3G on page 19
7.Reserve C238 for CRTDAC on page 10
8.Add R87 for Debug card on page 19
9.Change C108/C255 to 0.1uF for random hang issue
10.Change JP3 pin assignment on page 28
<10/21>
1. Update Power SCH
<10/29>
1. Audio AMP 10dB update to 6dB
<11/3>
1. Update Power SCH
<11/4>
1. Change R373、R374 to 56.2 ohm for DA-HP FSOV
2. Add C834、C851 for 3G noise
3. Change KB926 C1 to D2
4. Card reader RT5158E change to RT5159-GR
<11/5>
1. Swap D7 pin define
<11/10>
1. EC add R79、R90、R92 for SMS wakeup。

PVT-TEST Change

<11/28>
1. Reserve C40、C46、C47、C233
2. R617 change to 0ohm for RTS5159
3. R68 200K change to 100K for sequence
4. Remove C47
5. Add D30 for LVDS
6. Add C55 0.1U
7. U2 Change to SA000017B00
   -because RT9715 Can't protect

<12/30>
1. Update power MP SCH

MP Change

<1/21>
1. Change U1、U5、U6 to R3 P/N
2. Change R122、R123、R124、R125 to 2.2K
   for EC SMBUS rule
<2/6>
1. Combine N270 / N280 BOM

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